

CB-C8VX/VM 0.5-Micron Cell Based CMOS ASIC

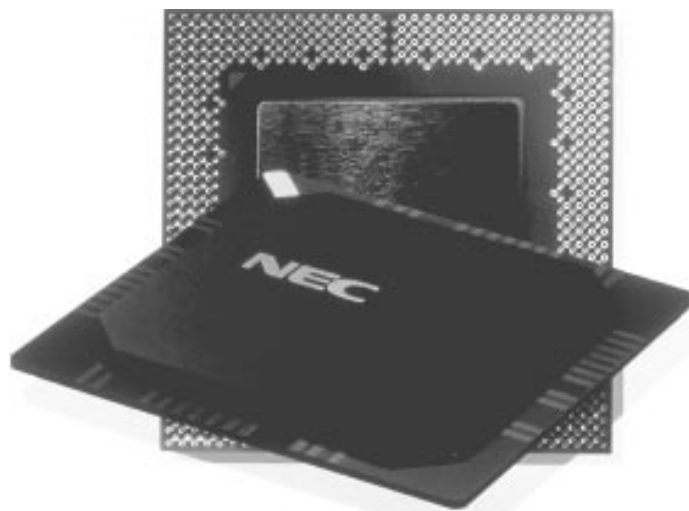
Description

NEC's CB-C8VX/VM family facilitates the design of complete cell-based silicon systems composed of user-defined logic, complex macrofunctions such as microprocessors, intelligent peripherals, analog functions and compiled memory blocks.

This cell based ASIC series employs a 0.5-micron (0.35 micron effective) silicon gate CMOS process with silicidation. This advanced process greatly reduces the number of contacts per cell, leading to area efficient library elements, optimised on speed at 3.3 V power supply. Finally, this results in an overall reduced power consumption per cell. Consequently, this technology combines the advantages of very high integration, high speed and low power consumption to cope with today's applications.

CB-C8VM, a derivate of CB-C8VX, features in addition a unique I/O structure, which provides a full 5 V CMOS interface.

CB-C8VX/VM are fully supported by NEC's sophisticated OpenCAD[®] Design Environment maximising design quality and design flexibility at the limits of the technology.



BGA Packages

Full 5 V CMOS Interface

CB-C8VM offers an interface to a 5 V signal environment. This is realised by implementing a section of thicker gate oxide into the I/O buffer, in order to guarantee the higher breakdown voltages. The 5 V I/O buffers can be placed at any location of the I/O area and are freely mixable with 3.3 V buffers. The internal core is identical to CB-C8VX.

CB-C8VX/VM Series Features	CB-C8VX/VM Series Benefits
• 0.5 micron (drawn) Ti-Silicide CMOS technology	• High density cell structure
• True 3.3 V process	• High speed at low power supply
• 36 base sizes, each with 2 and 3 metal layer	• Flexible base sizes to best fit design needs
• Usable gates from 13k to 890k	• High integration capabilities
• Full 5 V CMOS interface by multi-oxide I/O structure	• Supports flexible interfacing to different signal voltages
• Staggered pad ring for high gate to pad ratio	• Minimises device cost for high I/O requirements
• 5 V and 3.3 V PCI buffer	• Full PCI support compliant with latest PCI specification
• GTL and HSTL buffer in development	• High speed I/F to memory and processor busses
• Low power dissipation: 1.04 μ W/MHz/gate (3.3 V)	• Ideally suited for handheld applications
• Extensive macro range (CPUs, Peripherals, Analog)	• Advanced system on silicon capabilities
• Memory compiler for various types of memory blocks	• Area effective memory integration on chip
• Extensive package support: PQFP, TQFP, BGA, TBGA	• Delivers the latest package requirements
• Automatic clock skew control by Clock Tree Synthesis	• Minimises on-chip clock skew
• OpenCAD [®] - Popular, third party CAE tools supported	• Smooth design flow from customer design to silicon

Process

CB-C8VX/VM are manufactured using NEC's 0.5 µm drawn Titanium-Silicide CMOS process. This process allows to reduce the number of contacts between the diffusion layer and the metal layers, resulting into less inter-cell connections, which finally leads to an area efficient cell design.

Integration and Performance

Gate complexities of 890k usable gates can be integrated. All die sizes are routable with 2 or 3 metal layers. This gives enough flexibility to optimally fit design needs. Twenty-two die sizes are offering a single I/O pad ring and 14 are equipped with a staggered dual pad ring in order to achieve a high gate-to-pad ratio. For details, refer to table 1 and 2 below.

The family offers an extensive library of primitive macrofunctions characterised for 3.3 V operation. Each of these blocks has

several different drive strengths, allowing the synthesis tool to select the most suitable block for the required internal load. This generally reduces design overhead without influencing the design performance. The internal gate delay for a two-input NAND gate is 110 picoseconds (ps) (F/O = 1, l = 0 mm) and under loaded conditions 220 ps (F/O = 2, l = 2 mm).

To meet today's high speed demands, high performance I/O macros are mandatory. CB-C8VX/VM supports macros like GTL, HSTL for fast, low power data transfer, PCI signalling standards as well as PLLs to synchronise chip-to-chip system clocks. Also, CB-C8VX/VM offers a variety of macrofunctions to be incorporated on a single chip. These macrofunctions include, CPU cores, peripheral devices, RAM/ROM and analog functions, enabling designers to perform Systems on Silicon.

Step Name	I/O	Usable Gates ¹⁾	
		2 Layer	3 Layer
B18	88	13640	21823
B57	104	19588	31341
B97	120	26764	42823
C37	136	35059	56094
C76	152	44272	70835
D16	168	54779	87647
D55	184	66161	105858
D75	192	72382	115811
E15	208	85662	137059
E54	224	99760	159617
E94	240	115253	184405
F34	256	131864	210983
F74	272	149228	238764
G14	288	168052	268883
G53	304	187584	300134
G93	320	208622	333795
H33	336	230777	369243
H72	352	253574	405718
J32	376	290546	464873
J71	392	316059	505695
K11	408	343200	549120
K90	440	400237	640379

Table 1: CB-C8VX/VM die sizes (single pad ring)

¹⁾ Glue logic only design, with average utilisation

Step Name	I/O	Usable Gates ¹⁾	
		2 Layer	3 Layer
B73T	148	19588	31341
C37T	188	31607	50571
C50T	196	34354	54966
D01T	228	46487	74380
D52T	260	60452	96723
D90T	284	72128	115404
E54T	324	93876	150202
F18T	364	118486	189578
F70T	396	140235	224375
G34T	436	169996	271993
H49T	508	230777	369243
J51T	572	292588	469141
K92T	660	389541	623265
M97T	788	555287	888459

Table 2: CB-C8VX/VM die sizes (dual pad ring)

¹⁾ Glue logic only design, with average utilisation

Low Power Consumption

NEC's CB-C8VX/VM Ti-Silicide process features exceptionally low power dissipation to facilitate high-speed operation without the need of costly package options, and drastically increases battery-life for handheld applications. At 3 V, this ASIC family dissipates 0.9 μ W per gate and MHz, at 3.3 V 1.04 μ W/gate/MHz.

Multi Voltage I/O Interface

For those systems not yet ready to migrate completely to 3.3 V, CB-C8VM has a full 5 V CMOS interface available. Applying two additional process steps, which realise a 'multi-oxide' section in the I/O area, 5 V speed and drive capabilities are available at the chip border with the help of a separate 5 V supply rail. The 5 V I/O buffers include level shifters to convert the 5 V signal levels down to the internal core supply voltage of 3.3 V. This CB-C8 derivate is called CB-C8VM and is, beside the different I/O structure, identical to CB-C8VX. In case the speed and drivability requirements of the 5 V I/O cells are moderate, CB-C8VX is flexible enough to offer as well 5 V tolerant I/Os, that safely interface to 5 V devices, avoiding the multi-oxide process steps and just using a single 3.3 V power supply.

	CB-C8VX	CB-C8VM
Device Names	μ PD97xxx	μ PD99xxx
Interface Options	<ul style="list-style-type: none"> • 3.3 V • 5 V tolerant 	<ul style="list-style-type: none"> • 3.3 V • 5 V tolerant • full 5 V
Core Voltage	3.3 V	3.3 V
I/O Voltage	3.3 V	3.3 V and 5 V

CB-C8VX/VM Interface Options

In both, CB-C8VX and VM the 3.3 V and 5 V interfaces can be mixed without restriction among the entire I/O ring.

System on Silicon

NEC offers a wide selection of CPU/MCU cores, industry standard intelligent peripheral macros, compilable RAM/ROM blocks as well as analog functions in hardmacro form that can be integrated onto a single chip. Including such macrofunctions in an ASIC design makes it possible to achieve a high level of integration, performance and system security.

Macro	Compatible Device	Description
NZ 70008H	μ PD70008A	Z80 - 8 bit Microprocessor (16MHz)
NZ V30MX	μ PD70108H	V30MX - 16 bit Microprocessor (16bit data bus, 33MHz)
NZ V810	μ PD70732	V810 - 32 bit RISC Microprocessor (25 MHz)
NZ V851	μ PD703000	V851 - 32 bit RISC Microcontroller
ARM7TDMI	ARM7TDMI	ARM7xxx 32 bit RISC Microprocessor family - derivatives on request
NZ 71037H	μ PD71037	Programmable DMA Controller (4 channels, 20MHz)
NZ 71051H	μ PD71051	USART - Serial Data Control (Full duplex Tx/Rx, 300kbit/s, 20MHz)
NZ 71054H	μ PD71054	Programmable Timer/Counter (16 bit, 3 counter, 6 modes, 20MHz)
NZ 71055H	μ PD71055	Programmable Parallel Interface (8 bit, 3 I/O ports, 3 modes)
NZ 71059H	μ PD71059	Programmable Interrupt Control (64 interrupt request inputs)
NA 4993	μ PD4993	8 bit Parallel I/O Real Time Clock
NA72065BL	μ PD72065B	Single/Double Density Floppy Disk Controller
NZ 72103	μ PD72103	HDLC Controller - Full duplex, Baud rate 4Mbps, built-in DMA
M I ² C	-	I ² C Bus Interface - Receive, Transmit, Master&Slave
NA 16450L	NS16C450	UART - For PC compatible serial ports
NA 16550L	NS16550A	UART with FIFO - For PC compatible serial ports

Table 3: Digital Macrofunctions

The range of NEC's on-chip macrofunctions includes for example NEC's proprietary 32 bit RISC CPU V810, ARM7TDMI one member of ARM's 32 bit RISC processor family, or V30MX an upgraded high speed version of the popular 16bit CPU V30HL, which operates at clock speeds of 33 MHz at 3.3 V, offers an improved 286-compatible address pipelining and uses a 24 bit address bus. Other specific cores can be implemented on request. For details on the on-chip macrofunctions, refer to table 3 and 4.

Embedded macrofunctions are easy to place, to route, and to simulate. Because these macros

are derived from NEC's standard parts, they have fully characterised parameters and can be tested with standard test vectors to ensure full functionality and reliability.

NEC's test bus architecture allows complete system simulation, production testing of the internal circuits of the macrofunctions as well as seamless emulation of embedded CPU cores. The CPU may be connected externally and can be replaced by an in-circuit emulator (ICE). Just two additional test control pins are required to perform this.

Macro	Description
AAAD8GPB	General Purpose A/D Converter - 8bit, 100ksps
ADA8GPB	General Purpose D/A Converter - 8bit, 100ksps
AAAD820B	High Speed A/D Converter - 8bit, 20Msps
AAD3830B	High Speed D/A Converter - Triple, 8bit, 30Msps, V-Output type
AADAA20B	High Speed D/A Converter - 10bit, 20Msps, V-Output type
AAD38M0B	High Speed D/A Converter - Triple, 8bit, 170Msps
AACP01UB	General Purpose Comparator, Response Time = 1us (max.)
AACP80NB	High Speed Comparator, Response Time = 80ns (max.)
AACP25NB	High Speed Comparator, Response Time = 25ns (max.)
AASWx1CB	Analog Switch for Input and Output, Frequency Response = 40MHz
AASWx1TB	Analog Through Switch for Input and Output
AZPLSLFB	Analog PLL -Frequency Multiplication, Output = 10-60MHz
AZPLSMFB	Analog PLL -Frequency Multiplication, Output = 60-110MHz
AZPLSHFB	Analog PLL -Frequency Multiplication, Output = 110-170MHz

Table 4: Analog Macrofunctions

Memory Macros

NEC's CB-C8VX/VM technology offers seven different memory types (see table 5), which optimally suit a particular application.

All memory blocks are realised as embedded hardmacros and are generated by a memory compiler. This compiler provides all libraries needed in the design flow, from front-end synthesis libraries to back-end physical layout libraries. To ease the task of RAM testing for the designer, NEC supplies standard test pattern sets, which help to save valuable development time.

Packaging

NEC offers a wide variety of over 60 package types, each best suited, depending on the characteristic criteria of pin count, density, size, assembly yield and cost. The CB-C8VX/VM family can be packaged in NEC's most popular surface-mount and through-hole packages. These include plastic quad-flat packs (PQFPs) with up to 376 pins. The QFP range includes thin packages (TQFP, LQFP) and QFPs with integrated heatspreader. Pin grid arrays (PGAs) with up to 528 pins and BGA or Tape BGA packages from 225 up to 696 pins can be used.

Macro Type	Word Range	Bit Range	Step Word / Bit
ROM	128 - 8192	4 - 64	128 / 2
Low Power RAM, Single-Port (Synchronous, Separate I/O)	64 - 512	1 - 32	16 / 1
	128 - 1024	1 - 16	32 / 1
	256 - 2048	1 - 8	64 / 1
High Density RAM, Single-Port (Synchronous, Separate I/O)	128 - 2048	1 - 64	32 / 1
High Speed RAM, Single-Port (Synchronous, Separate I/O)	32 - 2048	1 - 32	8 / 1
Register Files, Dual-Port	8 - 256	4 - 32	4 / 1
Register Files, Triple-Port	8 - 256	4 - 32	4 / 1

Table 5: Memory Blocks

CB-C8 Applications

CB-C8VX devices are targeted for 3.3 V products in telecommunications, electronic data processing (EDP) and consumer applications. Typical telecommunications applications include cellular telephones, high-end pagers and PCMCIA devices, as well as broad-band communication systems up to 156 Mbit/s. In the EDP segment, applications include personal computers, high-end workstations and mainframes, multimedia platforms, graphic cards, personal digital assistants (PDAs), notebook and pen-based devices, hand-held data-terminals and hard disk controllers. Consumer applications include games, video cameras, portable printers and sophisticated calculators.

Each of these applications demands the benefits of increased integration and low power consumption that only a cell-based family, using an optimised 3.3 V process technology can deliver. And wherever a full 5 V CMOS interface is required, CB-C8VM gives the flexibility.

Design Tool Support

The CB-C8VX/VM family is fully supported by NEC's OpenCAD[®] Design System, a unified front-to-back-end design package that allows designers to mix and match tools from the industry's most popular third-party vendors and from NEC's offering of powerful proprietary software tools. These tools perform schematic capture, logic synthesis, floor-planning, logic and timing simulation, layout, design and circuit rule check, and memory compilation.

The company's proprietary clock tree synthesis tool can be used to automatically buffer the clock lines as needed to minimise clock skew, essential for half-micron designs. The non-linear delay calculator ensures timing accuracy throughout the simulation, synthesis, and silicon stages. Finally, NEC's memory compiler software enables the generation of memory blocks based on size and performance requirements.

CB-C8VX/VM - Preliminary Electrical Characteristics

Absolute Maximum Ratings

Parameters	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	3.3V supply 5V supply	-0.5 to +4.6 -0.5 to +6.0	V
I/O voltage 3.3 V Interface Block 5 V Interface Block 5 V Swing Block	V_I/V_O		-0.5 to +4.6V and $V_I/V_O < V_{DD} + 0.5V$ -0.5 to +6.6V and $V_I/V_O < V_{DD} + 3.0V$ -0.5 to +6.0V and $V_I/V_O < V_{DD} + 0.5V$	V
Output Current	I_O	$I_{OL} = 1.0$ mA $I_{OL} = 2.0$ mA $I_{OL} = 3.0$ mA $I_{OL} = 6.0$ mA $I_{OL} = 9.0$ mA $I_{OL} = 12.0$ mA $I_{OL} = 18.0$ mA $I_{OL} = 24.0$ mA	3 7 10 20 30 40 60 80	mA
Operating temperature	T_{opt}		-40 to +85	°C
Storage temperature	T_{stg}		-65 to +150	°C

Recommended Operating Conditions ($T_a = -40$ to $+85$ °C)

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.3 V CMOS level 5.0 V CMOS level 5.0 V TTL level	3.0 4.5 4.75	3.3 5.0 5.0	3.6 5.5 5.25	V V V
Low-level input voltage	V_{IL}	3.3 V interface block 5 V interface block 5 V swing CMOS 5 V swing TTL	0 0 0 0		0.8 0.8 $0.3V_{DD}$ 0.8	V V V V
High-level input voltage	V_{IH}	3.3 V interface block 5 V interface block 5 V swing CMOS 5 V swing TTL	2.0 2.0 $0.7V_{DD}$ 2.0		V_{DD} 5.5 V_{DD} V_{DD}	V V V V
Positive trigger voltage	V_P	3.3 V interface block 5 V I/F(CMOS Schmitt) 5 V I/F(TTL Schmitt)	1.2 1.8 1.2		2.4 4.0 2.4	V V V
Negative trigger voltage	V_N	3.3 V interface block 5 V I/F(CMOS Schmitt) 5 V I/F(TTL Schmitt)	0.6 0.6 0.6		1.8 3.1 1.8	V V V

Recommended Operating Conditions (Ta = -40 to +85 °C)

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Hysteresis voltage	V _H	3.3 V interface block	0.3		1.5	V
		5 V I/F(CMOS Schmitt)	0.3		1.5	V
		5 V I/F(TTL Schmitt)	0.3		1.5	V
Input rise or fall time	t _r , t _f		0		200	ns
Input rise or fall time (Schmitt trigger input)	t _r , t _f		0		10	ms

DC Characteristics (V_{DD} = 3.3 ± 0.3 V, 5V ± 0.5 V, Ta = -40 to +85 °C)

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Static Current Consumption	I _{DDs}	V _I = V _{DD} B18 to H33			200	μA
		or GND H72 to K90			300	μA
Off-State Output Current	I _{OZ}	V _O = V _{DD} or GND			±10	μA
Output Short-Circuit Current	I _{OS}	V _O = 0 V			-250	mA
Input Leakage Current						
Normal Input	I _I	V _I = V _{DD} or GND		±10 ⁻⁵	±10	μA
With pull-up (50kΩ)	I _I	V _I = GND	-10	-40	-80	μA
With pull-up (5kΩ)	I _I	V _I = GND	-130	-350	-640	μA
With pull-down (50kΩ)	I _I	V _I = V _{DD}	10	65	130	μA
Input Leakage Current(5V)						
Normal Input	I _I	V _I = V _{DD} or GND		10 ⁻⁵	±10	μA
With pull-up (50kΩ)	I _I	V _I = GND	-15	-60	-130	μA
With pull-up (5kΩ)	I _I	V _I = GND	-195	-530	-980	μA
With pull-down (50kΩ)	I _I	V _I = V _{DD}	15	100	200	μA
Low Level Output Current						
• 3 V Interface		V _{OL} = 0.4 V				
3 mA	I _{OL}		3			mA
6 mA	I _{OL}		6			mA
9 mA	I _{OL}		9			mA
12 mA	I _{OL}		12			mA
18 mA	I _{OL}		18			mA
24 mA	I _{OL}		24			mA
• 5V Interface Buffer		V _{OL} = 0.4 V				
1 mA type	I _{OL}		1			mA
2 mA type	I _{OL}		2			mA
3 mA type	I _{OL}		3			mA
6 mA type	I _{OL}		6			mA
9 mA type	I _{OL}		9			mA

DC Characteristics ($V_{DD} = 3.3 \pm 0.3 \text{ V}$, $5\text{V} \pm 0.5 \text{ V}$, $T_a = -40 \text{ to } +85 \text{ }^\circ\text{C}$)

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Low Level Output Current						
• 5V Swing Buffer		$V_{OL} = 0.4 \text{ V}$				
1 mA type	I_{OL}		1			mA
2 mA type	I_{OL}		2			mA
3 mA type	I_{OL}		3			mA
6 mA type	I_{OL}		6			mA
9 mA type	I_{OL}		9			mA
12 mA type	I_{OL}		12			mA
18 mA type	I_{OL}		18			mA
High Level Output Current						
• 3.3 V Interface		$V_{OH} = 2.4 \text{ V}$				
3 mA	I_{OH}		-3			mA
6 mA	I_{OH}		-6			mA
9 mA	I_{OH}		-9			mA
12 mA	I_{OH}		-12			mA
18 mA	I_{OH}		-18			mA
24 mA	I_{OH}		-24			mA
• 5V Interface Buffer		$V_{OH} = 2.4 \text{ V}$				
1 mA type	I_{OH}		-1			mA
2 mA type	I_{OH}		-2			mA
3 mA type	I_{OH}		-2			mA
6 mA type	I_{OH}		-2			mA
9 mA type	I_{OH}		-2			mA
• 5V Swing Buffer		$V_{OH} = V_{DD} - 0.4 \text{ V}$				
1 mA type	I_{OH}		-1			mA
2 mA type	I_{OH}		-2			mA
3 mA type	I_{OH}		-3			mA
6 mA type	I_{OH}		-6			mA
9 mA type	I_{OH}		-9			mA
12 mA type	I_{OH}		-12			mA
18 mA type	I_{OH}		-18			mA
Low Level Output Voltage		$I_{OL} = 0 \text{ mA}$				
3.3 V Interface	V_{OL}				0.1	V
5 V Interface	V_{OL}				0.1	V
5 V Swing	V_{OL}				0.1	V
High Level Output Voltage		$I_{OH} = 0 \text{ mA}$				
3.3 V Interface	V_{OH}		$V_{DD} - 0.1$			V
5 V Interface	V_{OH}		$V_{DD} - 0.2$			V
5 V Swing	V_{OH}		$V_{DD} - 0.1$			V

AC Characteristics ($V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$, $5.5\text{ V} \pm 0.5\text{ V}$, $T_a = -40\text{ to } +85^\circ\text{C}$)

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Toggle frequency	f_{tog}	Internal toggle F/F (F/O = 2)		480		MHz
Propagation delay time	t_{PD}	Internal gate(F/O = 1, l = 1 mm)		0.23		ns
		Input buffer (F/O = 2, l = 2 mm)		0.37		ns
		Output buffer				ns
Output rise time	t_r	3.3V Interface ($C_L=15\text{pF}$, $I_{OL}=9\text{mA}$)		1.24		ns
		5V Swing ($C_L=15\text{pF}$, $I_{OL}=9\text{mA}$)		1.80		
Output fall time	t_r	3.3V Interface ($C_L=15\text{pF}$, $I_{OH}=-9\text{mA}$)		1.88		ns
		5V Swing ($C_L=15\text{pF}$, $I_{OH}=-9\text{mA}$)		1.91		
Output fall time	t_r	3.3V Interface ($C_L=15\text{pF}$, $I_{OH}=-9\text{mA}$)		1.32		ns
		5V Swing ($C_L=15\text{pF}$, $I_{OH}=-9\text{mA}$)		1.22		

Publications:

This data sheet contains a reduced set of information and operational data for CB-C8VX/VM cell based CMOS ASIC. The information in this document is subject to change without notice. Additional information is available in NEC's CB-C8VX/VM documentation. Please contact your local NEC Design Centre for further information.