

QB-8 / QB-8E 3.3 Volt , 0.44-Micron Gate-Array

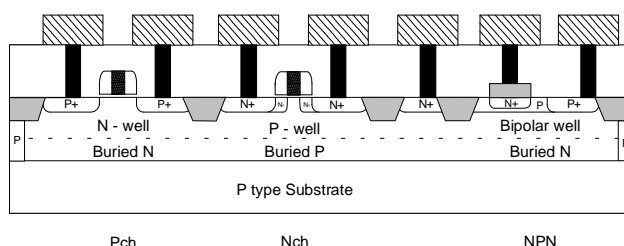
Description

NEC's 3.3V QB-8 family consists of ultra-high performance, sub-micron gate arrays, targeted for applications requiring high speeds and low power dissipation. The QB-8 family offers not only high speed but also low power dissipation and high density at a reasonable price. This combination of features is made possible through the use of a unique epi-less process that delivers the low cost and short manufacturing time of CMOS with the high speed of bipolar technology.

QB-8 is targeted for designs in advanced network and data communications, industrial applications, telecommunications, and computing applications such as engineering workstations, high-end personal computers, mainframes and high-speed peripherals.

The device processing include a 0.44-micron silicon-gate technology and three-layer metalization produced in NEC's 0.5-micron CMOS fabrication line. This technology features channelless (sea-of-gate) architecture with an internal gate-delay of 107 ps (F/O=1, L=0mm) and power dissipation of 1 μ W/MHz/gate at 100% switching rate. The high performance I/O macros include LVTTL,

Figure 1. Cross Section of QB-8



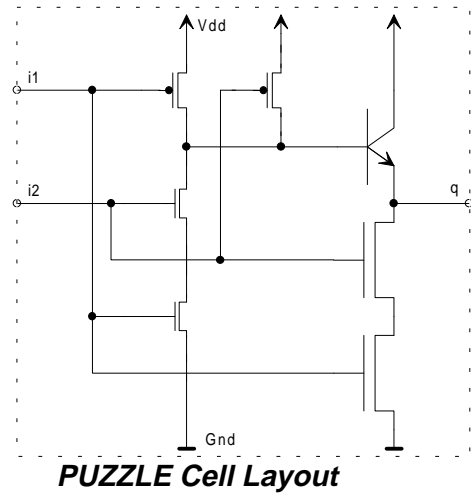
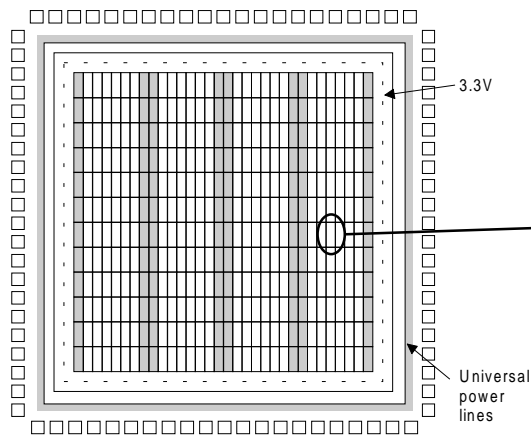
GTL, HSTL, p-ECL and LVDS. PCI signalling standards are also supported including 3.3V 66MHz PCI. This technology is enhanced by a set of advanced features including phase-locked loops, clock tree synthesis, and high speed memories.

The QB-8 family consists of 11 masters, offered in densities of 33K to 382K raw gates. The gate array family is supported by NEC's OpenCAD design system; a mixture of popular third-party CAE tools, and proprietary NEC tools. NEC proprietary tools include clock tree synthesis for clock skew minimisation, and table look-up delay calculator for accurate delay calculation.

Table 1. QB-8 Series Features and Benefits

QB-8 Series Features	QB-8 Series Benefits
<ul style="list-style-type: none"> • 0.44-micron (drawn), 3 level metal process • BiNMOS process does not use epitaxial layer • "PUZZLE" cell architecture with mixed transistor sizes • 11 base arrays with raw gates from 33K to 382K gates • Embedded array option (QB-8E) • Optimized I/O cell size • PCI, GTL, HSTL, p-ECL, LVDS interface blocks • Low power dissipation of 1 μW/MHz/gate • Clock tree synthesis tool • Table look up simulation models 	<ul style="list-style-type: none"> ⇒ Delivers bipolar speed at CMOS turn-around time / cost ⇒ Shortens turn-around time and reduced production costs ⇒ Superior timing behaviour with respect to fan-out ⇒ Many base arrays allow good fit to user's requirements ⇒ NEC on chip logic macros running with up to 622 MHz ⇒ Enables high-speed I/O buffers in only one I/O slot ⇒ I/O transfer rate up to 250 MHz (622 MHz in QB-8E) ⇒ Delivers support for ultra-high-speed communications ⇒ Automatic insertion of low skew clock tree ⇒ Allows extreme accurate timing verification

Figure 2. Chip Layout & Cell Configuration



Array Architecture

The QB-8 family is built with NEC's 0.44-micron channelless array architecture. The array is divided into I/O and core regions (see Figure 2). The I/O regions contain input and output buffers. The core region contains the sea-of-gates array. The QB-8 gate arrays architecture provides extra flexibility for high performance system designs. The arrays contain several power rails; a 3.3V rail, and power rails for special I/O types, such as 5V PCI, HSTL, GTL, and p-ECL.

Core Architecture

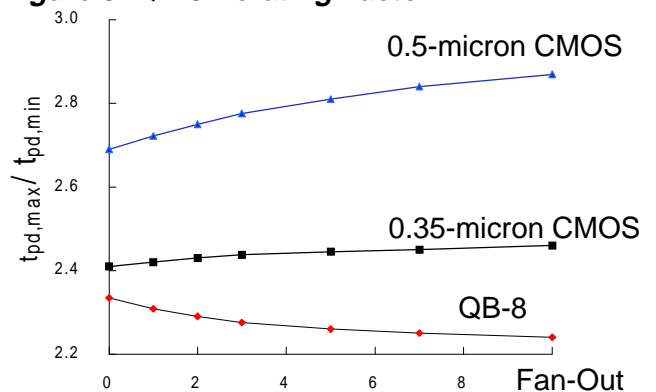
QB-8 uses a proprietary architecture called PUZZLE. It combines three different size transistors into a single, highly dense architecture tightly interlocked as in a puzzle. The result is an ASIC that uses small CMOS transistors for low input capacitance and signalling within a macro, and bipolar transistors for high driveability and signalling between macros.

The core region consists of an array of gates. Each cell contains 4 n-channel and 2 p-channel transistors and 1 vertical bipolar npn-transistor. One cell is equivalent to one 2-input NAND gate (L302). The logic transistors are sized to offer a superior ratio of speed to silicon area.

Performance

The QB-8 family basic performance characteristics of power dissipation and minimum gate delay are positioned very close to NEC's 0.35-micron CMOS ASIC family at a price level only slightly above NEC's 0.5-micron CMOS family. Moreover the real advantages of this gate array family can be seen in conjunction with cell loads. Typically the derating factor ($t_{PD,MAX}/t_{PD,MIN}$) increases with fanout for pure CMOS technology, but the QB-8 family shows a decrease. So QB-8 offers higher performance stability despite fluctuations in environmental conditions.

Figure 3. QB-8 Derating Factor



The increased driving capability of QB-8 leads to significant reduced load dependency of the gate delay.

The tradeoff of this superior performance is an increased quiescent current compared to pure CMOS technology. Nevertheless power dissipation is much smaller than known from conventional BiCMOS logic arrays, as the dynamic power consumption is very similar to comparable CMOS devices.

Although the quiescent current is about 10 times larger than the static current of a comparable CMOS device, the total power consumption for a 150kGate design running with 33 MHz and a switching rate of 33% is only 1% higher compared to a pure CMOS solution (see also Fig. 4).

Gate Array Sizes

The 11 available QB-8 masters cover a wide range of complexity as shown in table 2. The gate density is about 30% higher compared to 0.5-mircon CMOS gate array. Due to reduced wiring capacity this results in an increased timing performance. The QB-8 family uses three metal layer for signal routing.

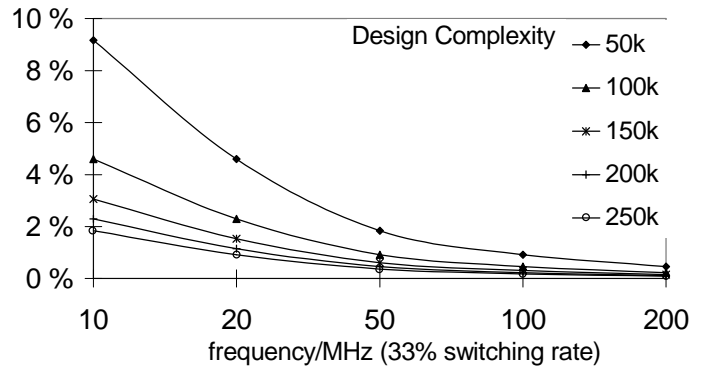
Table 2. QB-8 Master Devices

Device	Available Gates	Usable ¹ Gates	I/O Pads ²
μPD67821	32832	22982	156
μPD67822	44352	31046	180
μPD67823	56800	39760	204
μPD67824	69520	48664	224
μPD67825	93184	65229	260
μPD67826	123808	86666	300
μPD67827	136752	95726	316
μPD67828	167280	117096	348
μPD67829	234320	164024	412
μPD67830	292896	205027	460
μPD67831	381840	267288	524

¹ Actual gate utilisation varies depending on circuit implementation

² Depending on package and circuit specification, some pads are used for power only and are not available as signal pads.

Figure 4. Increase of Power of QB-8 with respect to CMOS technology (reference: CMOS-9)



Macro and Block Library Support

The QB-8 block library which is compatible to the CMOS gate array block library includes a full set of basic functions.

The QB-8 family macro library includes a complete set of CMOS I/O buffers. Furthermore LVTTTL, GTL, HSTL, pECL, PCI and LVDS I/O buffers are supported.

The memory macro library contains asynchronous single and dual port high-speed RAM also as single port high-density RAM .

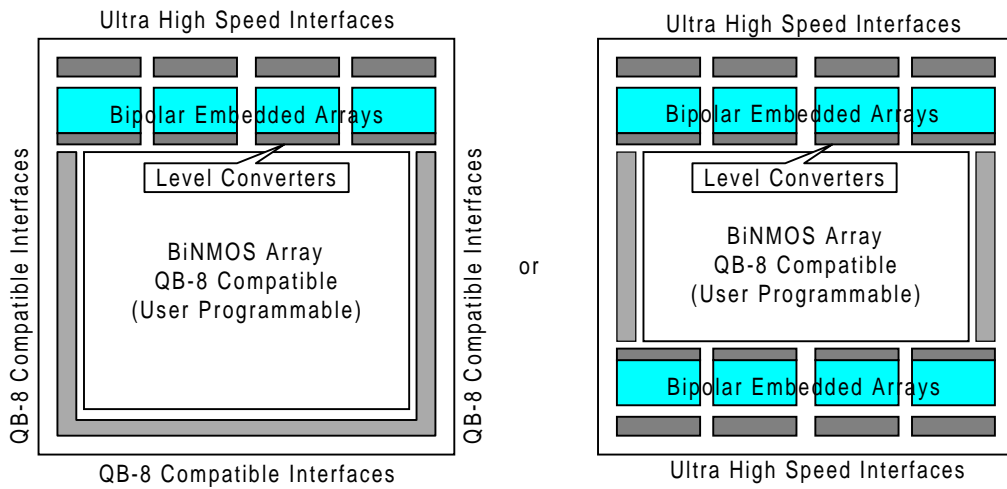
Table 3. QB-8 Memory Macros

RAM-Type	RAM-Size
High-speed dual port	32 - 512 words 8 - 32 bits
High-speed single port	32 - 512 words 8 - 32 bits
High-density RAM	32 - 4096 words 4 - 40 bits

Further macro support for special functions from NEC's megafunction library is available on request.

As the list of available macro functions is rapidly growing please contact your local NEC design center for latest information.

Figure 5. QB-8E Embedded Hard Macros (configuration examples)



Embedded Array Option QB-8E

QB-8E is a special process option of the QB-8 family, which allows embedding predefined macros in the standard gate array. While in standard CMOS embedded array structures the focus application is the integration of high density RAM, the main focus of QB-8E is the integration of ultra high speed function blocks.

The QB-8E macros include ultra high speed bipolar macros as 622 MHz I/O cells, 622 MHz parallel/serial converter and 622 MHz PLL. Moreover the embedded macro structure is ideally suited for integration of accurate programmable delay macros and analog bipolar macros, such as a bandgap voltage reference. The maximum toggle frequency in embedded CML (Common Mode Logic) Flip-Flop macros is about 1.7 GHz with a power dissipation of about 0.8 mW independent of the operating frequency.

Additional embedded macros for the QB-8E family will be developed by NEC on customers request.

5V I/O Interfacing

Although the QB-8 family is based on a true 3.3 V process, it supports mixed 3.3V/5V systems. The I/O library includes a complete set of 5V tolerant I/O buffers, working with a single 3.3V supply voltage. Using these I/O cells makes it possible to connect QB-8 designs directly to 5V TTL compatible I/O's.

Table 4. QB-8E Embedded Macros ¹

Macro	Description
P/S Converter	Parallel/serial converter n:1(n=4,8,12,16) - Operating Frequency: 622 MHz - Power Dissipation: 115 mW (n=8)
S/P Converter	Serial/parallel converter 1:n(n=4,8,12,16) - Operating Frequency: 622 MHz - Power Dissipation: 115 mW (n=8)
CTS PLL	Multiply Clock Synthesizer PLL - Multiplier: 4x, 8x, 12x, 16x, 32x - Operating Frequency: 622 MHz ± 6% - Phase Jitter: ±50 ps
CR PLL	Clock Recovery PLL - Operating Frequency: 622 MHz
Delay70	Variable Delay Macro - Program resolution: 10 bit, - Span: 7 ns (min) variable delay, - Resolution: 25 ps (worst)
Delay35	Variable Delay Macro - Program resolution: 9 bit, - Span: 3.5 ns (min) variable delay, - Resolution: 25 ps (worst)
PECL	3.3V-PECL 100k/ECL 100k compatible - Differential/single ended line interface - Operating Frequency: 622 MHz Power Dissipation: - 1.7 mW for input - 23.14 mW single ended output - 50.5 mW diff. ended high speed output - 38.01 mW diff. ended low power output

¹ other macros are available on customer request

QB-8 Applications

Applications for NEC's QB-8 ASIC family are widespread and mainly make use of the very good cost/performance ratio in general or the superior timing performance especially of the QB-8E subfamily. The trade-offs which have to be taken into account are the limited circuit complexity which currently limits the system on silicon integration and the static supply current, which makes QB-8 less suitable for battery supplied applications.

So the focus applications are transmission and switching applications, for example STM-1 transceiver, STM-4 transceiver and ATM-switches. Furthermore QB-8 ASIC's are well suited for automated test equipment (ATE) systems and electronic measuring systems, which also take advantage of the reduced influence of the environment conditions. In the same way high speed bus applications in the field of engineering work stations (EWS) can take advantage of QB-8. Due to the reasonable price QB-8 is also interesting for a wide range of high speed consumer products.

And finally QB-8 is able to replace many conventional BiCMOS applications with a significant reduction of cost and power consumption.

CAD Support

The QB-8 family ASIC's are completely supported by NEC's OpenCAD™ design environment, a unified front-to-back-end design package that allows designers to mix and match tools from the industry's most popular third-party vendors and from NEC's offering of powerful proprietary software tools. These tools perform schematic capture, logic synthesis, floor-planning, logic and timing simulation, layout, design and circuit rule check, and memory compilation.

The company's proprietary clock tree synthesis tool can be used to automatically buffer the clock lines as needed to minimise clock skew, essential for high speed designs.

The library elements of NEC's QB-8 family are modelled in a non-linear way using table look up methods. This allows the most accurate timing verification throughout synthesis, estimated timing simulation and sign-off timing simulation as it includes not only the influence of actual load conditions but also of the logic-cells input slopes. NEC spends most efforts to guarantee a converging design flow and to avoid design iterations.

Placement and routing is performed in NEC's European headquarters in Düsseldorf (Germany), which allows quick and flexible handling of specific design demands. In most cases no floorplanning is necessary, to meet the required timings. This leads to a significant reduction of design efforts on the customer's side.

Test Support

The QB-8 family supports automatic test generation through a scan-test methodology, which allows higher fault coverage, easier testing and shorter development time. This includes internal scan as well as boundary scan. NEC also offers optional build-in self test (BIST) architecture for RAM testing. If no BIST is implemented, NEC delivers a complete set of test-patterns for RAM test.

Packaging

NEC offers a wide variety of over 60 package types. The QB-8 family can be packaged in NEC's most popular surface-mount and through-hole packages. These include plastic quad-flat packs (PQFPs). Pin grid arrays (PGAs) and Ball grid array (BGA) packages are also supported.

Publications

This data sheet contains specifications, package information, and operational data for the QB-8 gate array families. Additional design information is available in NEC's ASIC selection guide, QB-8 block library and QB-8 design manual. Contact your local NEC Design Center for further information.

Absolute Maximum Ratings

Power supply voltage, V_{DD}	-0.5 to 4.6 V
Input voltage, V_I	
3V input buffer (at $V_I < V_{DD} + 0.5$ V)	-0.5 to 4.6 V
3V fail-safe input buffer (at $V_I < V_{DD} + 0.5$ V)	-0.5 to 4.6 V
5V-tolerant buffer (at $V_I < V_{DD} + 3.0$ V)	-0.5 to 6.6 V
Output voltage, V_O	
3V buffer (at $V_O < V_{DD} + 0.5$ V)	-0.5 to 4.6 V
5V-tolerant buffer (at $V_O < V_{DD} + 3.0$ V)	-0.5 to 6.6 V
Latch-up current, I_{LATCH}	>1 A (typ)
Operating temperature, T_{OPT}	-40 to +85°C
Storage temperature, T_{STG}	-65 to +150°C

Input/Output Capacitance

$V_{DD}=V_I=0$ V; $f=1$ MHz

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	20	pF
Output	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	10	20	pF

Note:

(1) Values do not include package pin capacitance.

Power Consumption

Description	Limits	Unit
Internal Cell	1.09	μ W/MHz
Input block (FI01)	6.92	μ W/MHz
Output block (F002 @ 15 pF)	260	μ W/MHz

Recommended Operating Conditions

Parameter	Symbol	3V Buffer		5V-Tolerant		3.3V PCI		5V PCI		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Power supply voltage	V_{DD}	3.0	3.6	3.0	3.6	3.0	3.6	3.0	3.6	V
Junction temperature	T_J	-40	+125	-40	+125	-40	+125	-40	+125	°C
Low-level input voltage	V_{IL}	0	0.8	0	0.8	-0.5	0.3 V_{DD}	-0.5	0.8	V
High-level input voltage	V_{IH}	2.0	V_{DD}	2.0	V_{DD}	0.5 V_{DD}	$V_{DD}+0.5$	2.0	$V_{DD}+0.5$	V
Input rise or fall time	t_R, t_F	0	200	0	200	0	200	0	200	ns
Input rise or fall time, Schmitt	t_R, t_F	0	10	0	10	0	200 ns	—	—	ms

AC Characteristics

$V_{DD} = 3.3$ V \pm 0.3 V; $T_J = -40$ to +125°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency	f_{TOG}	670			MHz	D-F/F; F/O = 1
Delay time						
2-input NAND (F322)	t_{PD}		90		ps	F/O = 1; L = 0 mm
	t_{PD}		106		ps	F/O = 2; L = typ
Flip-flop (F611)	t_{PD}		463		ps	F/O = 1; L = 0 mm
	t_{PD}		492		ps	F/O = 2; L = typ
	t_{SETUP}	540			ps	—
	t_{HOLD}	10			ps	—
Input buffer (FI01)	t_{PD}		211		ps	F/O = 1; L = 0 mm
	t_{PD}		220		ps	F/O = 2; L = typ
Output buffer (12 mA) 3.3V	t_{PD}		925		ps	$C_L = 0$ pF
Output buffer (12 mA) 3.3V	t_{PD}		2136		ps	$C_L = 50$ pF
Output buffer (12 mA) 5V-tolerant	t_{PD}		TBD		ps	$C_L = 0$ pF, 50 pF
Output buffer (6 mA) 5V-tolerant	t_{PD}		1004		ps	$C_L = 0$ pF
Output buffer (6 mA) 5V-tolerant	t_{PD}		2158		ps	$C_L = 50$ pF
Output rise time (9 mA)	t_R		920		ps	$C_L = 15$ pF
Output fall time (9 mA)	t_F		680		ps	$C_L = 15$ pF

DC Characteristics

$V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $T_J = -40 \text{ to } +125^\circ\text{C}$

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent current						
$\mu\text{PD67831, 67830}$	I_{DDS}		15	4800	μA	$V_I = V_{\text{DD}}$ or GND
$\mu\text{PD67829, 67828, 67827}$	I_{DDS}		9	3000	μA	$V_I = V_{\text{DD}}$ or GND
$\mu\text{PD67826, 67825, 67824}$	I_{DDS}		5	1500	μA	$V_I = V_{\text{DD}}$ or GND
$\mu\text{PD67823, 67822, 67821}$	I_{DDS}		2	700	μA	$V_I = V_{\text{DD}}$ or GND
Off-state output leakage current						
3V output	I_{OZ}			± 10	μA	$V_O = V_{\text{DD}}$ or GND
5V-tolerant output	I_{OZ}			± 14	μA	$V_O = V_{\text{DD}}$ or GND
Output sink current with pull-up ($V_O = 3\text{V}$)	I_{R}			14	μA	$V_{\text{PU}} = 5.5\text{V}$, $R_{\text{PU}} = 2\text{k}\Omega$
Output sink short circuit current	I_{OS}			-250	mA	$V_O = \text{GND}$
Input leakage current						
Regular	I_{I}			± 10	μA	$V_I = V_{\text{DD}}$ or GND
50 k Ω pull-up	I_{I}	-30	-66	-144	μA	$V_I = \text{GND}$
5 k Ω pull-up	I_{I}	-300	-660	-1440	mA	$V_I = \text{GND}$
50 k Ω pull-down	I_{I}	30	66	144	μA	$V_I = V_{\text{DD}}$
Pull-up resistor						
50 k Ω pull-up	R_{PU}	25.0	50.0	100.0	k Ω	
5 k Ω pull-up	R_{PU}	2.5	5.0	10.0	k Ω	
50 k Ω pull-down	R_{PD}	25.0	50.0	100.0	k Ω	
Low-level output current						
3V buffers						
3 mA (F009)	I_{OL}	3			mA	$V_{\text{OL}} = 0.4 \text{ V}$
6 mA (F004)	I_{OL}	6			mA	$V_{\text{OL}} = 0.4 \text{ V}$
9 mA (F001)	I_{OL}	9			mA	$V_{\text{OL}} = 0.4 \text{ V}$
12 mA (F002)	I_{OL}	12			mA	$V_{\text{OL}} = 0.4 \text{ V}$
18 mA (F003)	I_{OL}	18			mA	$V_{\text{OL}} = 0.4 \text{ V}$
24 mA (F006)	I_{OL}	24			mA	$V_{\text{OL}} = 0.4 \text{ V}$
5V-tolerant buffers						
1 mA (FV0A)	I_{OL}	1			mA	$V_{\text{OL}} = 0.4 \text{ V}$
2 mA (FV0B)	I_{OL}	2			mA	$V_{\text{OL}} = 0.4 \text{ V}$
3 mA (FV09)	I_{OL}	3			mA	$V_{\text{OL}} = 0.4 \text{ V}$
6 mA (F002)	I_{OL}	6			mA	$V_{\text{OL}} = 0.4 \text{ V}$
Low-level output voltage						
3V buffers	V_{OL}			0.1	V	$I_{\text{OL}} = 0 \text{ mA}$
5V-tolerant buffers	V_{OL}			0.1	V	$I_{\text{OL}} = 0 \text{ mA}$
High-level output voltage						
3V buffers	V_{OH}	$V_{\text{DD}} - 0.1$			V	$I_{\text{OH}} = 0 \text{ mA}$
5V-tolerant buffers	V_{OH}	$V_{\text{DD}} - 0.2$			V	$I_{\text{OH}} = 0 \text{ mA}$

