Design Services

Product Letter

CAD

Static Timing Analysis & Postlayout Timing Fix

Description

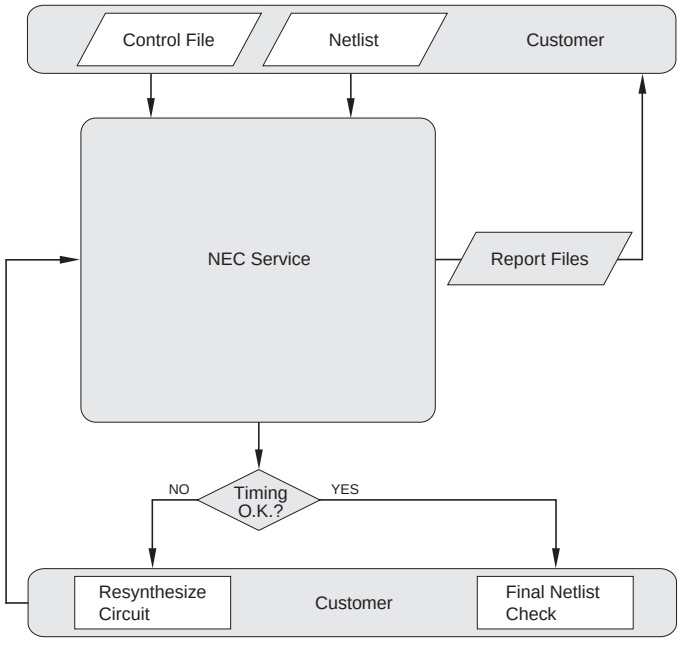
In deep submicron designs the impact of the wire gets more and more important and has to be taken into account already during initial logical synthesis. This is done by using appropriate wireload models. The wireload models estimate the load of a net according to the macrosize and the fanout of the net. This estimation reflects reality quite well, but still there can be some nets which are longer than estimated after placement and routing is done. If these nets are part of a timing critical path of the design, postlayout timing violations may occur. The purpose of the Postlayout Optimization is to fix these violations. During this task only parts which contribute to timing violations are touched. All other parts, which already fulfill the timing remain unchanged. These modifications are recognized during layout and only incremental modifications are made (ECO, Engineering Change Order).
Extensive tool and flow knowledge is necessary to cope with remaining timing violations after layout. Lack of expertise and resources within the design team could result in schedule slippage and missed deadlines. The critical design step of postlayout timing fix often requires assistance by tool experts.

NEC´s design service team meets the need for engineering assistance during this project stage. By providing experienced engineering resources for postlayout STA (Static Timing Analysis) and postlayout optimization, NEC´s design service can help to keep projects on schedule.

STA & Postlayout Optimization Benefits

- Accelerates design completion by providing implementation and verification resources
- Minimizes project risk through expert assistance during postlayout timing fix
- Project success through in-house design expertise and outsourced STA and postlayout optimization expertise

Service Flow



System@IC
Solutions on a Chip

NEC

Service Details

Target Customers

Customers with limited STA and optimization expertise within NEC´s design flow and immediate project needs are excellent candidates for NEC´s STA and postlayout optimization services. For example, a project team which focuses mainly on system definition and implementation rather than dealing with timing behaviour of the circuit after layout, can rely on NEC´s services. Customers benefit from close and local link to NEC´s Frontend and Backend team.

Prerequisites

Prerequisites for STA and Postlayout Optimization Services include:

- Complete toplevel constraint file (Synopsys DC script format or write_script output file)
- DIF (Design Information File, please refer to ***1**)
- Electric Design Rule Checker Result File (GateDRC report without errors)
- Target design (fulfils NEC´s prelayout design rules)
- Customer team with design knowledge to answer design specific requests

***1** DIF file specification in NEC´s OpenCAD Online Documentation

STA & Postlayout Optimization Service Deliverables

The STA/Postlayout Optimization Service deliverables include:

- Providing an Application Note how to constrain digital circuits in Synopsys Design Compiler environment
- Providing an Application Note about STA and postlayout optimization within NEC´s design flow
- Kickoff meeting with customer (optional)
- Netlist with fixed postlayout timing violations based on customer constraint file
- Corresponding back-annotation data after layout (SDF and caps file)
- Static Timing Analysis reports based on postlayout SDF and customer constraints
- Set of customized wireload models based on initial layout data (optional, for resynthesis purposes)

The exact deliverables may be modified through the mutual consent of NEC and the customer.

Included Tasks

The basic service package includes the following tasks, performed on a single chip design:

- Perform prelayout electrical design rule check
- Perform prelayout Static Timing Analysis based on customer constraints and estimated database
- Perform postlayout Static Timing Analysis based on customer constraints and SDF from layout
- Fix of postlayout timing violations with automatic or manual modifications
- Functional verification of circuit after postlayout timing fix (formal verification)

Optional:

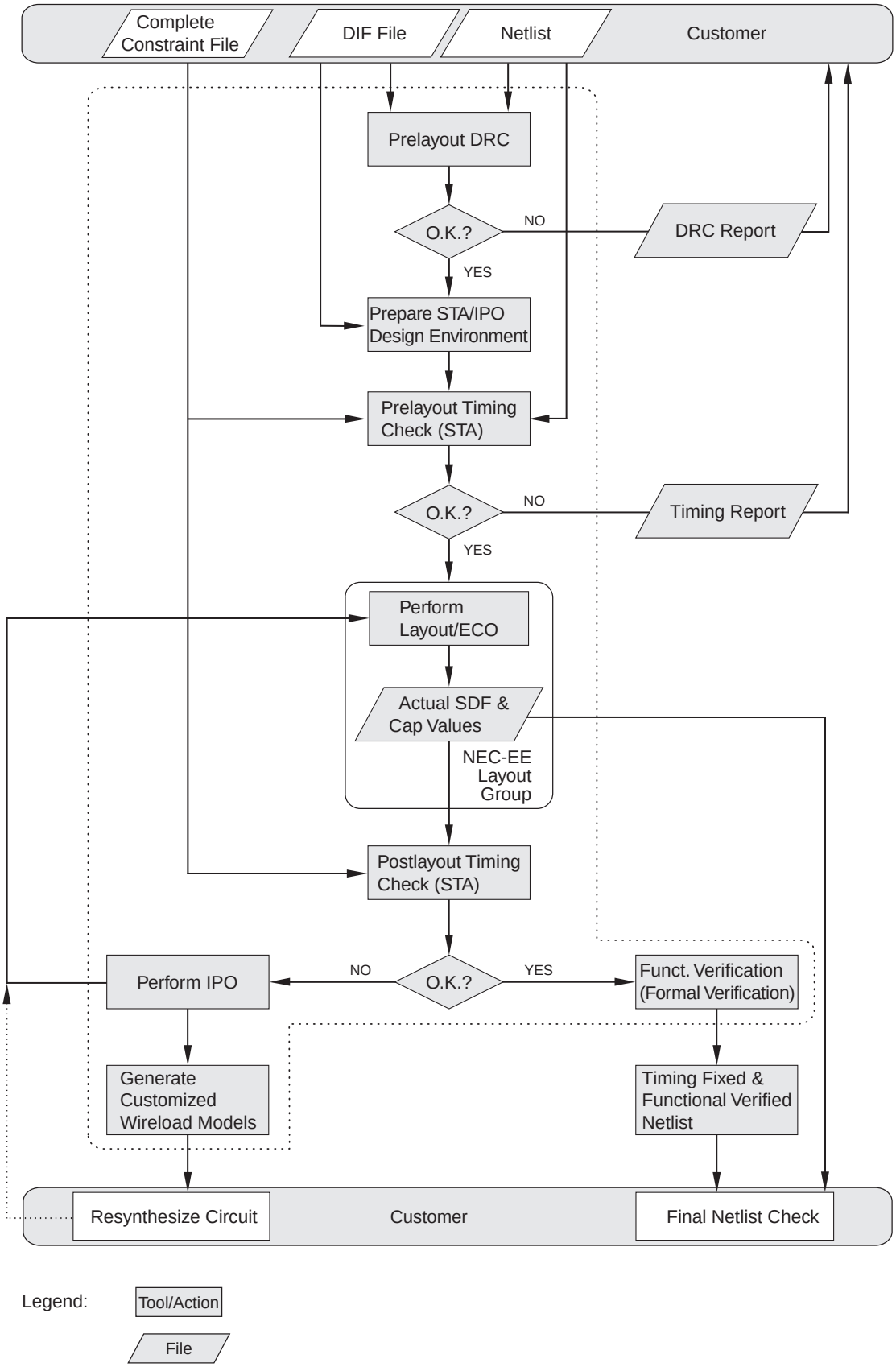
- Generation of customized wireload models for resynthesis purposes

Whom to Contact

For detailed discussion on NEC´s STA and Postlayout Optimization Services, contact your local NEC ASIC sales or application office.

For further information on other NEC products visit our European website at **www.nec.de**

STA and Postlayout Optimization Flow (detailed)



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With compliments