AGENDA

- Synergy Hardware Concepts
- Synergy Design Philosophy
- Synergy Compatibility & Scalability
- Synergy IP focus
- Q&A
What is Synergy?

A complete and qualified platform that accelerates embedded development, inspiring innovation and enabling differentiation.

Our Three Values

- Faster Time to Market
- Reduce Total Cost of Ownership
- Lower Barriers to Entry
Synergy Hardware Concepts

• Synergy is the first ARM based general purpose microcontroller family from Renesas

• Designed from the beginning as a scalable platform

• Reuses proven Renesas IP

• Enhanced and new peripheral IP blocks to meet the needs of the embedded market
ARM Implementation
Cortex M Series

- Synergy devices use Cortex-M cores
  - Cortex-M4 with single precision FPU (CM4F)
    - ARMv7E-M Architecture
  - Cortex-M0+ (CM0+)
    - ARMv6-M Architecture

- In addition to “Core CPU”, additional ARM licensed IP
  - Nested Vectored Interrupt Controller (NVIC)
  - ARM Memory Protection Unit (MPU)
  - Debugger Subsystem (CoreSight)
  - System Tick Timer (SysTick)
Cortex M Series within Synergy

- How much can we do at once?
Synergy Design Philosophy
Synergy Design Philosophy within Synergy Portfolio

Flash Density vs. Pin Count Graph

- Flash Density:
  - 4M
  - 3M
  - 2M
  - 1M
  - 512K
  - 256K
  - 128K
  - 64K

- Pin Count:
  - 36
  - 48
  - 64
  - 100
  - 121
  - 144/145
  - 176
  - 224

Legend:
- S1
- S3
- S5
- S7
Synergy Process Technology

130nm MF3

Ultra-Low Power
Core Frequency
Up to 32MHz

Ultra-Low Power
Core Frequency
Up to 32MHz

High Efficiency
Core Frequency
33-100MHz

High Efficiency
Core Frequency
33-100MHz

40nm RV40F

High Integration
Core Frequency
101-200MHz

High Integration
Core Frequency
101-200MHz

High Performance
Core Frequency
201-300MHz

High Performance
Core Frequency
201-300MHz
Synergy Package Scalability

Scalability Within Series..

S1, S3 Package Types:

- 145-pin LGA
- 64-pin QFN
- 36, 40, 48, 64, 100, 144-pin LQFP
Synergy Package Scalability

- A closer look at 64, 100, 144-pin packages:
Synergy Package Scalability

- Similarly, on the right hand side of 64, 100, 144-pin packages
Synergy Package Scalability

Scalability within Series...

S5, S7 Package Types:

- 145, 176, 224 LGA
- 100, 144, 176 LQFP
Synergy Package Scalability

- S7 & S5 have 100 pin and 144 pin LQFP
- S3 has 100 pin and 144 pin LQFP

- These are compatible, process technology permitting.
Synergy Package Scalability – Between Series

S7 / S5 (RV40F)

S3 (MF3)
Synergy Package Scalability
# Synergy Peripheral Compatibility

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<th>Memory</th>
<th>Clock</th>
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<th>Analog</th>
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<td>240MHz CPU</td>
<td>Flash: 2MB-4MB</td>
<td>Sampling Rate Converter</td>
<td></td>
<td></td>
<td>Graphic LCD controller w/ 2D accelerator</td>
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<td>External Memory I/F (SDRAM)</td>
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<td><strong>High Integration RV40F S5</strong></td>
<td>120MHz CPU</td>
<td>Flash:128KB-2MB</td>
<td>HOCO 16/18/20 MHz</td>
<td>USB 2.0 HS Host/Peripheral/ OTG</td>
<td>TSIP AES 256 SHA1, SHA2 RNG</td>
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<td>Cortex M0+</td>
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<td>HOCO 24 - 64 MHz</td>
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<td>GHASH AES 128/256 TRNG</td>
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## Synergy Peripheral Compatibility

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<td>RAM:512KB/64 0KB</td>
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<td><strong>Cortex M4</strong></td>
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<td><strong>High Efficiency MF3 S3</strong></td>
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<td>GPT: 32b</td>
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<td></td>
<td><strong>ECC on Flash</strong></td>
<td><strong>Sub Clock 32.768 kHz</strong></td>
<td>Main clock 1-20MHz</td>
<td>Sub Clock 32.768 kHz</td>
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<td>Parity on RAM</td>
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</tbody>
</table>

**Clock:**
- LOCO 32.768 kHz for WDT
- LOCO 15 kHz for WDT
- Main clock 1-20MHz
- Sub Clock 32.768 kHz

**Processor:**
- Cortex M0+
- Cortex M4
- Cortex M0

**Memory:**
- Flash: 2MB-4MB
- RAM:512KB/64 0KB
- Data Flash: 64KB
- Flash: 128KB-2MB
- RAM:16KB-640KB
- Data Flash: 16-32KB
- Flash: 768KB-1MB
- RAM:16KB-192KB
- Data Flash: 16KB
- Flash: 8KB-128KB
- RAM:4KB-32KB
- Data Flash: 4KB
- ECC on Flash
- Parity on RAM

**Digital I/O:**
- GPIO
- UART
- SPI
- I2C
- CAN
- SDHI/SDIO
- QSPI
- MMC
- NAND
- NOR
- ESD
- Memory
- I2C
- CAN
- SPI
- UART
- USB
- Ethernet
- SD
- SDHC
- SDXC

**Clock:**
- Main clock 1-20MHz
- Sub Clock 32.768 kHz

**Security:**
- ECC on Flash
- Parity on RAM
- MPU (Renesas)

**Analog:**
- ADC
- DAC
- Comparator
- Sensor
- Power

**Miscellaneous:**
- WDT
- iWDT
- DTC, DMA
- CAN
- POR
- LVD
- GPIO
- Illegal Memory access
- Debug Trace
- MPU (Renesas)
# Synergy Peripheral Compatibility

## High Performance RV40F S7
- **CPU**: 240MHz CPU
- **Memory**: Flash: 2MB-4MB, RAM: 512KB-640KB, Data Flash: 64KB
- **Clock**: PLL HOCO, HOCO 18/16/20 MHz
- **Comm.**: USB 2.0 FS (host/Peripheral/OTG)
- **Timer**: GPT: 32b
- **Security**: GHASH AES 128/256, SHA1, SHA2
- **User Interface**: Cap Touch
- **Analog**: Regulator (Linear)
- **Safety**: WDT
- **System**: External Memory I/F (SRAM)

## High Integration RV40F S5
- **CPU**: 120MHz CPU
- **Memory**: Flash: 12KB-2MB, RAM: 16KB-640KB, Data Flash: 16-32KB
- **Clock**: PLL HOCO, HOCO 16/18/20 MHz
- **Comm.**: USB 2.0 HS Host/Peripheral/OTG
- **Timer**: TSIP AES 128/192256 SHA1, SHA2
- **Security**: TRNG
- **User Interface**: Graphic LCD controller w/ 2D accelerator
- **Analog**: DAC: 12b
- **Safety**: Comparator: 6 channel
- **System**: External Memory I/F (SRAM)

## High Efficiency MF3 S3
- **CPU**: Cortex M4
- **Memory**: Flash: 76KB-1MB, RAM: 16KB-192KB, Data Flash: 16KB
- **Clock**: PLL
- **Comm.**: USB 2.0 FS (host/Periph/OTG)
- **Timer**: GPT: 32b
- **Security**: GHASH AES 128/256, TRNG
- **User Interface**: Segment LCD 52x8 max
- **Analog**: Regulator (Linear)
- **Safety**: WDT
- **System**: External Memory I/F (SRAM)

## Low Power MF3 S1
- **CPU**: Cortex M0+
- **Memory**: Flash: 8KB-128KB, RAM: 4KB-32KB, Data Flash: 4KB
- **Clock**: HOCO 24-64 MHz, LOCO 32.768 kHz
- **Comm.**: USB 2.0 FS (Peripheral)
- **Timer**: GPT: 32b, GPT: 16b
- **Security**: GHASH AES 128/256, TRNG
- **User Interface**: MPU (Renesas)
- **Analog**: MPU (ARM), Vref
- **Safety**: Debug Trace
- **System**: Illegal Memory access

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Synergy Peripheral Compatibility

**S1**

- **RTC implementation**
  - BUS INTERFACE
  - Sub-Clock LOCO
  - Clock Divider
  - Calendar Count
  - Interrupt Controller
  - Reduced Alarm Function

**S7**

- **RTC implementation**
  - BUS INTERFACE
  - Sub-Clock LOCO
  - Clock Divider
  - Calendar Count
  - Interrupt Controller
  - Alarm Function
  - Time Capture

- **RTCCRy**
- **RMONCPy**

### Important Points
- Physical features of the peripheral in the S1 MCU is a pure orthogonal subset of the features in the S7 MCU.
- The control registers have no dependencies as they are scaled down to a lower feature set.
- The control register address offsets are constant even as features are removed.

### Register Addresses

- **R64CNT**
- **RYRCNT**
- **RSECAR**
- **RYRAREN**
- **RCR1**
- **RADJ**
- **RTCCRy**
- **RMONCPy**
Synergy IP
Synergy IP – Compressed..
Synergy IP: Proven technology

- DMAC/DTC
- RTC
- WDT/iWDT
- CGC/CAC/DOC
- USB/Ethernet
- CAN/RIIC/RSPI
- DAC
- I2S/SRC
- ISI – Image Sensor Interface
- CTC – Capacitive Touch Controller
- SLCD – Segment LCD Controller
Synergy IP: Proven technology - Enhanced

- ELC - Event Link Controller
- IOPC - I/O Port Control
- ADC
- SCI - Serial Communication Interface
- CRC
- SD/MMC Controller
Synergy IP: New MCU technology

- HMI : GLCDC/2D-DRW/JPEG
- SCEx - Secure Crypto Engine
- QSPI - QuadSPI Serial Flash Interface
- MMF - Memory Mirror Function
- Information Memory
- RMPU - Renesas Memory Protection Unit collection
- AGT - Asynchronous General Purpose Timer
- GPTx / POE / OPS - General PWM Timer / Port Output Enable / Output Phase Switching
Synergy IP Highlights
Graphics LCD Controller (GLCDC)

- Supports alpha-blended background and 2x layers
- Layers up to 800x480x32bpp
- Many Layer formats
- 1bpp CLUT to 32bpp ARGB8888
- Layers sourced from internal RAM/Flash or external SDRAM
- SDRAM 16bits x 120Mhz
- High function output control
- Brightness, Contrast, Dither, Gamma
- Configurable control pins (HS,VS,DEN)
2D Drawing Engine (DRW) (7,5)

Module to update the frame buffer with graphical content to off load CPU
Supports a variety of 2D graphics including lines, circles, ellipses, polygons, custom geometry, etc.

**Drawing Features**

**Vector Drawing**
- Allows for easier implementation of edge anti-aliasing and blurring with reduced overhead
- Uses half plane rendering approach
- Can be used to combine non-linear, quadratic equation-based primitives (conic sections, quadratic curves, etc.)

**BitBLT (Bit Boundary Block Transfer)**
- Allows combination of two bitmaps; for example, combining a rectangle and a texture.
- Results in fill, copy, rotate, scale, alpha blending, color conversion, bilinear filtering, etc.

**Vector Image**  
**Raster Image** (Aliased)  
**Anti-aliased Image**

**Anti-Aliasing**

Engine can achieve results 20x faster than CPU

Simplified rendering setup showing efficient decoupling of CPU (for other system tasks) & 2D Drawing Engine (for graphics rendering)
JPEG Codec (7,5)

Hardware accelerator for JPEG encode/decode

Supports streaming of source and destination data

Fast decode permits MJPEG

20x faster than CPU

Supports subsampling for thumbnails and simple scaling

Pixel Formats

- **Compression**
  - YCbCr422 (H = 2:1:1, V = 1:1:1)

- ** Decompression**
  - YCbCr444 (H = 1:1:1, V = 1:1:1)
  - 8 lines by 8 pixels minimum coded unit for each decompression
  - YCbCr422 (H = 2:1:1, V = 1:1:1)
  - 8 lines by 16 pixels MCU
  - YCbCr411 (H = 4:1:1, V = 1:1:1)
  - 8 lines by 32 pixels MCU
  - YCbCr420 (H = 2:1:1, V = 2:1:1)
  - 16 lines by 16 pixels MCU
  - Output pixel format ARGB8888, RGB565

Simplified implementation of JPEG Codec
QuadSPI Serial Flash Interface (QSPI)

- Dedicated serial memory interface
- Normal operation maps read requests into MCU Linear Memory
- QSPI provide 64Mbyte window serial memory
- For S7 device running 4-bit data and 60Mhz clocking
- Sequential accesses
- Faster than 80ns 16-bit parallel NOR flash
- Eliminates external bus in many applications
- Great for bulk graphics resource storage
- Code can also be executed directly from this space
- Erase and programming operations
- Available through QSPI “direct mode”
Memory Mirror Function (MMF)

- Physical address in Flash can be mapped to a virtual address in memory map by write to a single register

Benefits:
- Supports safe firmware updates - Multiple versions of application firmware can be held in Flash
- Switch instantly between firmware version images - No need to copy new firmware image to specific link location
- No requirement to build firmware for position independent code (PIC)
Memory Mirror Function (MMF)

- Simple hardware implementation and easy to use in application firmware

![Synergy MCU Diagram]
Information Memory (Factory Flash)

- Programmed in read-only flash area at final test
- Product Information
  - Unique ID (128 bits)
  - Part Number and Product Marking (ASCII 32 characters)
  - Part Data (package, pin count, temperature spec, etc)
- Peripheral Data
  - Base address, channel count, version for every peripheral
  - Availability in package of ports, ADC, CTSU, etc
- Memory type, start, size
- Firmware API to simplify access and future version updates
- Synergy Framework will utilize to become “smarter”
General PWM Timer (GPTx)

- Scalable family of timers to meet application needs and costs
  - GTU16: 16bit timer unit with timer/capture/compare/count/motor
  - GTU32: TU16 functions with 32bit registers
  - GTU32E: TU32 functions with additional high end motor control
  - GTU32EHx: TU32x functions with pico second delay comparators

Event Sources:
- 2x I/O pins per channel
- Up to 8x ELC events shared across all channels
- Events can cause TUx to start/stop/clear/count/capture
- TUx channels can be assigned to larger groups for multi-channel functions (inverter control)
- Up to 4x TUx POE pins that are shared across all channels
## Comparison Between GPTs

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<th>GPT32-E</th>
<th>GPT32</th>
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<td>PCLK (/4, /16, /64, /256, /1024)</td>
<td>PCLK (/4, /16, /64, /256, /1024)</td>
<td>PCLK (/4, /16, /64, /256, /1024)</td>
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<tr>
<td>3-Phase PWM Generator</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
</tr>
<tr>
<td>Pico Second Delay</td>
<td>Available</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Available In</td>
<td>S7</td>
<td>S5</td>
<td>S7</td>
<td>S1</td>
</tr>
</tbody>
</table>
Asynchronous General Purpose Timer (AGT) (7,5,3,1)

True asynchronous behavior, does not rely on PCLK active

Modes of operation

- **Timer mode**
  - Count source is counted

- **Pulse Output mode**
  - Count source is counted and output is inverted upon timer underflow

- **Event Counter mode**
  - An external event is counted

- **Pulse Width Measurement mode**
  - An external pulse width is measured

- **Pulse Period Measurement mode**
  - An external pulse period is measured

Widely selectable count sources: LOCO, SUBOsc, PCLK, external

Can operate in standby modes (and wake system)

Works on Vbatt on S3 devices

Simplified implementation of Asynchronous General Purpose Timer
Memory Protection Unit collection

- Multiple needed to get the job done
MPU Collection

- ARM MPU
- Cortex Standard MPU
- Provides access rights for up to 8x regions
- Only protects access from CPU
- Aware of processor operations
  - Execute .vs Data, Read .vs Write, Privileged .vs User
- Regions are “blocky”
- Requires RTOS support for full benefit
MPU Collection

- Bus Master MPU
- Renesas MPU

- Only applies to Non-CPU masters
- Provides fine control of bus master memory accesses
  - When disabled, all memory is considered read/write
  - When enabled, all memory is protected (only enabled areas accessible)
- Address ranges fine grained (32-bit boundaries)
- Configuration based on driver requirements…examples:
  - Limit EDMAC to configured buffers
  - Limit DTC/DMAC to some peripheral areas and buffers
  - Limit HMI to video buffers, resources and scratchpad
MPU Collection

- Bus Slave MPU
- Renesas MPU

- Provides permission for a master to access a slave…

Examples:
- Prevent DMAC/DTC from accessing external bus
- Prevent HMI from accessing flash
- Address ranges are inherent in what is blocked
- Simple configuration based on application requirements
- Done once at startup
MPU Collection

- Synergy Microcontrollers are designed to be highly scalable and compatible
- Include all the peripherals you need, with enhancements to well-proven Renesas IP
- And a few ‘gems’ that I hopefully have given you a glimpse of!
THANK YOU FOR YOUR ATTENTION

PLEASE REMEMBER TO COMPLETE THE FEEDBACK SURVEY IN YOUR SMARTPHONE APP
## Synergy MCU S7 Series

### 240-MHz ARM® Cortex®-M4 CPU

<table>
<thead>
<tr>
<th>Memory</th>
<th>Analog</th>
<th>Timing &amp; Control</th>
<th>System &amp; Power Mgmt</th>
<th>Security &amp; Encryption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code Flash (4 MB)</td>
<td>12-Bit A/D Converter x2 (25 ch.)</td>
<td>General PWM Timer 32-bit</td>
<td>DMA Controller (8 ch.)</td>
<td>128-bit Unique ID</td>
</tr>
<tr>
<td>Data Flash (64 KB)</td>
<td>12-Bit D/A Converter x2</td>
<td>Enhanced High Resolution x4</td>
<td>Event Transfer Controller</td>
<td>TRNG</td>
</tr>
<tr>
<td>SRAM (640 KB)</td>
<td>High-Speed Analog Comparator x6</td>
<td>General PWM Timer 32-bit</td>
<td>Low Power Modes</td>
<td>AES (128/192/256)</td>
</tr>
<tr>
<td>Flash Cache</td>
<td>PGA x6</td>
<td>Enhanced x4</td>
<td>Switching Regulator</td>
<td>3DES/ARC4</td>
</tr>
<tr>
<td>Security MPU</td>
<td>Temperature Sensor</td>
<td>General PWM Timer 32-bit x6</td>
<td>Multiple Clocks</td>
<td>RSA/DSA</td>
</tr>
<tr>
<td>Memory Mirror Function</td>
<td></td>
<td>Asynchronous General Purpose Timer x2</td>
<td>Port Function Select</td>
<td>SHA1/SHA224/SHA256</td>
</tr>
</tbody>
</table>

### Connectivity
- Ethernet MAC Controller x2
- Ethernet DMA Controller
- Ethernet PTP Controller
- USB HS
- CAN x2
- SPI x2
- QSPI x2
- IIC x3
- SSI x2
- SDHI/MMC x2
- Sampling Rate Converter
- IrDA Interface
- External Memory Bus

### System & Power Mgmt
- DMA Controller (8 ch.)
- Data Transfer Controller
- Event Link Controller
- Low Power Modes
- Switching Regulator
- Multiple Clocks
- Port Function Select
- RTC
- SysTick

### Safety
- ECC in SRAM
- SRAM Parity Error Check
- Flash Area Protection
- ADC Diagnostics
- Clock Frequency Accuracy
- Measurement Circuit
- CRC Calculator
- Data Operation Circuit
- Port Output Enable for GPT
- IWDT

### Security & Encryption
- 128-bit Unique ID
- TRNG
- AES (128/192/256)
- 3DES/ARC4
- RSA/DSA
- SHA1/SHA224/SHA256
- GHASH
### Synergy MCU S5 Series

**120-MHz ARM® Cortex®-M4 CPU**

<table>
<thead>
<tr>
<th>Memory</th>
<th>Analog</th>
<th>Timing &amp; Control</th>
<th>HMI</th>
<th>Security&amp;Encryption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code Flash (2 MB)</td>
<td>12-Bit A/D Converter x2 (21 ch.)</td>
<td>General PWM Timer 32-bit Enhanced High Resolution x4</td>
<td>Capacitive Touch Sensing Unit (18 ch.)</td>
<td>128-bit Unique ID</td>
</tr>
<tr>
<td>Data Flash (64 KB)</td>
<td>12-Bit D/A Converter x2</td>
<td>General PWM Timer 32-bit Enhanced x4</td>
<td>Graphics LCD Controller</td>
<td>TRNG</td>
</tr>
<tr>
<td>SRAM (640 KB)</td>
<td>High-Speed Analog</td>
<td>General PWM Timer 32-bit</td>
<td>2D Drawing Engine</td>
<td>AES (128/192/256)</td>
</tr>
<tr>
<td>Flash Cache</td>
<td>Comparator x6</td>
<td>Asynchronous General Purpose Timer x2</td>
<td>JPEG Codec</td>
<td>3DES/ARC4</td>
</tr>
<tr>
<td>Security MPU</td>
<td>PGA x6</td>
<td>WDT</td>
<td>Parallel Data Codec Capture</td>
<td>RSA/DSA</td>
</tr>
<tr>
<td>Memory Mirror Function</td>
<td>Temperature Sensor</td>
<td></td>
<td></td>
<td>SHA1/SHA224/ SHA256</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>GHASH</td>
</tr>
</tbody>
</table>

**Connectivity**

- Ethernet MAC Controller
- Ethernet DMA Controller
- Ethernet PTP Controller
- USBHS
- USBFS
- CAN x2
- SDHI/MMC x2
- Serial Communications Interface x10
- IrDA Interface
- QSPI
- SPI x2
- IIC x3
- SSI x2
- Sampling Rate Converter
- External Memory Bus

**System & Power Mgmt**

- DMA Controller (8 ch.)
- Data Transfer Controller
- Event Link Controller
- Low Power Modes
- Multiple Clocks
- Port Function Select
- RTC
- SysTick

**Safety**

- ECC in SRAM
- SRAM Parity Error Check
- Flash Area Protection
- ADC Diagnostics
- Clock Frequency Accuracy Measurement Circuit
- CRC Calculator
- Data Operation Circuit
- Port Output Enable for GPT
- IWDT

- WDT

- 128-bit Unique ID
- TRNG
- AES (128/192/256)
- 3DES/ARC4
- RSA/DSA
- SHA1/SHA224/ SHA256
- GHASH
# Synergy MCU S3 Series

**48-MHz ARM® Cortex®-M4 CPU**

<table>
<thead>
<tr>
<th>Memory</th>
<th>Analog</th>
<th>Timing &amp; Control</th>
<th>HMI</th>
<th>Connectivity</th>
<th>System &amp; Power Mgmt</th>
<th>Safety</th>
<th>Security &amp; Encryption</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code Flash (1 MB)</td>
<td>14-Bit A/D Converter (28 ch.)</td>
<td>General PWM Timer 32-bit x10</td>
<td>Capacitive Touch Sensing Unit (35 ch.)</td>
<td>USBFS</td>
<td>DMA Controller (4 ch.)</td>
<td>ECC in SRAM</td>
<td>128-bit Unique ID</td>
</tr>
<tr>
<td>Data Flash (16 KB)</td>
<td>12-Bit D/A Converter x2</td>
<td>Asynchronous General Purpose Timer x2</td>
<td>Segment LCD Controller</td>
<td>CAN</td>
<td>Data Transfer Controller</td>
<td>SRAM Parity Error Check</td>
<td>TRNG</td>
</tr>
<tr>
<td>SRAM (192 KB)</td>
<td>Low-Power Analog Comparator x2</td>
<td></td>
<td></td>
<td>SDHI/MMC</td>
<td>Event Link Controller</td>
<td>Flash Area Protection</td>
<td>AES (128/256)</td>
</tr>
<tr>
<td>Flash Cache</td>
<td>High-Speed Analog Comparator x2</td>
<td>Low Power Modes</td>
<td></td>
<td>IrDA Interface</td>
<td>Low Power Modes</td>
<td>ADC Diagnostics</td>
<td>GHASH</td>
</tr>
<tr>
<td>Security MPU</td>
<td>OPAMP x4</td>
<td>Multiple Clocks</td>
<td></td>
<td>QSPI</td>
<td>Port Function Select</td>
<td>Clock Frequency Accuracy</td>
<td></td>
</tr>
<tr>
<td>Memory Mirror Function</td>
<td>Temperature Sensor</td>
<td>Port Function Select</td>
<td></td>
<td>SPI x2</td>
<td>RTC</td>
<td>Measurement Circuit</td>
<td></td>
</tr>
</tbody>
</table>

## Connectivty
- USBFS
- CAN
- SDHI/MMC
- Serial Communications Interface x6
- IrDA Interface
- SPI x2
- IIC x3
- SSI x2
- External Memory Bus

## System & Power Mgmt
- DMA Controller (4 ch.)
- Event Link Controller
- Low Power Modes
- Multiple Clocks
- Port Function Select
- RTC
- SysTick

## Safety
- ECC in SRAM
- SRAM Parity Error Check
- Flash Area Protection
- ADC Diagnostics
- Clock Frequency Accuracy
- Measurement Circuit
- CRC Calculator
- Data Operation Circuit
- Port Output Enable for GPT
- IWDT

## Security & Encryption
- 128-bit Unique ID
- TRNG
- AES (128/256)
- GHASH

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# Synergy MCU S1 Series

## Memory
- Code Flash (128 KB)
- Data Flash (4 KB)
- SRAM (16 KB)

## Analog
- 14-Bit A/D Converter (18 ch.)
- 12-Bit D/A Converter
- Low-Power Analog Comparator x2
- Temperature Sensor

## Timing & Control
- General PWM Timer 32-bit
- General PWM Timer 16-bit x6
- Asynchronous General Purpose Timer x2
- WDT

## System & Power Mgmt
- Data Transfer Controller
- Event Link Controller
- Low Power Modes
- Multiple Clocks
- Port Function Select
  - RTC
  - SysTick

## Safety
- SRAM Parity Error Check
- Flash Area Protection
- ADC Diagnostics
- Clock Frequency Accuracy Measurement Circuit
- Data Operation Circuit
- CRC Calculator
- Port Output Enable for GPT
- IWDT

## Connectivity
- USBFS
- CAN
- Serial Communications Interface x3
  - SPI x2
  - IIC x2

## HMI
- Capacitive Touch Sensing Unit (32 ch.)

## Security & Encryption
- 128-bit Unique ID
- TRNG
- AES (128/256)
<table>
<thead>
<tr>
<th>Core</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPU</td>
</tr>
<tr>
<td>ARM MPU</td>
</tr>
<tr>
<td>NVIC</td>
</tr>
<tr>
<td>ETM</td>
</tr>
<tr>
<td>JTAG</td>
</tr>
<tr>
<td>SWD</td>
</tr>
<tr>
<td>Boundary Scan</td>
</tr>
</tbody>
</table>

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ARM® Cortex®-M4 Integration (7)

Ultra-high performance and high integration
Maximum system clock frequency: 240 MHz

Performance
- CoreMark™/MHz: 3.28 @ 200 MHz
- CoreMark™ at maximum system frequency: 681 @ 240 MHz

ARM® v7E-M architecture profile
- High code density with 32-bit performance
- Low gate count
- Thumb-2 instruction set

17 core registers
- 13 general purpose registers
- Stack pointer, link register, program counter, program status registers

Bit-banding support

Floating Point Unit
- 32-bit instructions for single-precision (C float) data-processing operations
- Multiply and accumulate instructions for increased precision (fused MAC)
**ARM® Cortex®-M4 Integration (5)**

Ultra-high performance and high integration
Maximum system clock frequency: 100 MHz – 200 MHz

**Performance**
- CoreMark™/MHz: TBD
- CoreMark™ at maximum system frequency: TBD

ARM® v7E-M architecture profile
- High code density with 32-bit performance
- Low gate count
- Thumb-2 instruction set
- 17 core registers
  - 13 general purpose registers
  - Stack pointer, link register, program counter, program status registers

Bit-banding support
Floating Point Unit
- 32-bit instructions for single-precision (C float) data-processing operations
- Multiply and accumulate instructions for increased precision (fused MAC)

**ARM® Cortex®-M4 CPU integration**
in Synergy MCUs
**ARM® Cortex®-M4 Integration (3)**

Ultra-high performance and high integration
Maximum system clock frequency: 48 MHz

Performance
- CoreMark™/MHz: 3.31 @ 48 MHz
- CoreMark™ at maximum system frequency: 158.9 @ 48 MHz

ARM® v7E-M architecture profile
- High code density with 32-bit performance
- Low gate count
- Thumb-2 instruction set
- 17 core registers
- 13 general purpose registers
- Stack pointer, link register, program counter, program status registers
- Bit-banding support

Floating Point Unit
- 32-bit instructions for single-precision (C float) data-processing operations
- Multiply and accumulate instructions for increased precision (fused MAC)
ARM® Cortex®-M0+ Integration (1)

Maximum system clock frequency: 32 MHz
Performance
- CoreMark™/MHz: 2.49 @ 32 MHz
- CoreMark™ at maximum system frequency: 79.8 @ 32 MHz
- ARM® v6-M architecture profile
- High code density with 32-bit performance
- Low gate count
- Supports Thumb and many Thumb-2 subset instructions
- 19 core registers
  - 13 general purpose registers
  - Stack pointer, link register, program counter, program status register, control, priority mask
- Optimized for ultra-low power
- Power control of system components
- Integrated sleep modes
- Fast code execution permits longer sleep time
- Optimized code fetching reduces flash and ROM power consumption
- Deterministic, high-performance interrupt handling
- Single-cycle IO access
- Single-cycle hardware integer multiplier

ARM® Cortex®-M0+ CPU integration in Synergy MCUs
ARM® Cortex®-M4 NVIC and ARM® MPU (7,5)

Nested Vector Interrupt Controller (NVIC)
- Provides configurable interrupt-handling abilities to the processor
- Facilitates low latency exception and interrupt handing
- Controls power management using Wake-up Interrupt Controller (WIC)
- Supports 96 interrupts
- Enables tail-chaining
- Supports priority grouping
- Level-sensitive and pulse-sensitive interrupts

ARM® Memory Protection Unit (ARM® MPU)
- Supports ARMv7 Protected Memory System Architecture model
- 8 protect regions (0-7 priority)
- Access permissions
- Generates a fault if restricted area of memory is accessed
- Use to enforce privilege rules, to separate processes, and to enforce access rules

ARM® Cortex®-M4 CPU integration in Synergy MCUs
**ARM® Cortex®-M4 NVIC and ARM® MPU (3)**

Nested Vector Interrupt Controller (NVIC)
- Provides configurable interrupt-handling abilities to the processor
- Facilitates low latency exception and interrupt handing
- Controls power management using Wake-up Interrupt Controller (WIC)
- Supports 64 interrupts
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ARM® Memory Protection Unit (ARM® MPU)
- Supports ARMv7 Protected Memory System Architecture model
- 8 protect regions (0-7 priority)
- Access permissions
- Generates a fault if restricted area of memory is accessed
- Use to enforce privilege rules, to separate processes, and to enforce access rules

**ARM® Cortex®-M4 CPU integration in Synergy MCUs**
ARM® Cortex®-M0+ NVIC (1)

Nested Vector Interrupt Controller (NVIC)
- Provides configurable interrupt handling abilities to the processor
- Supports up to 32 external interrupts
- Dedicated non-maskable interrupt (NMI) pin
- Level-sensitive and pulse-sensitive interrupts
- Vector table can be relocated.
ARM® Cortex®-M4 Debug (7,5)

JTAG and Serial Wire Debug (SWD) port
- Uses CoreSight™ Debug Access Port (DAP)
- Provides debug access to all memory and registers in the system, memory-mapped devices, internal core, and debug control registers
- JTAG interface maximum speed: 25 MHz
- SWD interface maximum speed: 25 MHz

Flash patch and breakpoint
- Use to implement hardware breakpoints
- Patches code and data from code space to system space
- 6 instruction comparators
- 2 literal comparators
**ARCM Cortex-M4 Debug (3)**

JTAG and Serial Wire Debug (SWD) port
- Uses CoreSight™ Debug Access Port (DAP)
- Provides debug access to all memory and registers in the system, memory mapped internal core, and debug control registers
- JTAG interface maximum speed: 25 MHz
- SWD interface maximum speed: 25 MHz

Flash patch and breakpoint
- Use to implement hardware breakpoints
- Patches code and data from code space to system space
- 6 instruction comparators
- 2 literal comparators

**ARM® Cortex®-M4 CPU integration in Synergy MCUs**
ARM® Cortex®-M0+ Debug (1)

CoreSight™ Debug Access Port (DAP)
- Provides a 25-MHz serial wire debug port
- Full system-level debug access

Breakpoint and Watch Unit
- Use to implement breakpoints and watchpoints
- 4 instruction comparators
- 2 comparators for watchpoints

Debug registers
- Reset control
- Halt control

CoreSight™ ETB-M0 +
- Revision: r0p1-00rel0
- MTB RAM: 1 KB

ARM® Cortex®-M0+ Processor

ARM® Cortex®-M0+ CPU integration in Synergy MCUs
ARM® Cortex®-M4 Trace (7,5)

CoreSight™ Embedded Trace Macrocell and Buffer (ETM and ETB)
- Useful for instruction trace
- CoreSight™ ETM™-M4
- Revision: r0p1-00rel0
- ARM ETM architecture version 3.5
- Embedded trace buffer (ETB)
- ETB RAM: 2 KB

Trace Port Interface Unit (TPIU)
- Bridge ETM and ITM to a data stream required by a trace port analyzer (TPA)
- Can output data in 4-bit serial wire output format

Data Watchpoint Trace (DWT)
- Use to implement watchpoints, data tracing, and system profiling
- 4 comparators for watchpoints and triggers

CoreSight™ Instrumentation Trace Macrocell (ITM)
- Supports printf style debugging to trace operating systems
- Generates diagnostic system information

ARM® Cortex®-M4 CPU integration in Synergy MCUs
**ARM® Cortex®-M4 Trace (3)**

CoreSight™ Embedded Trace Macrocell and Buffer (ETM and ETB)
- Useful for instruction trace
- CoreSight™ ETM™-M4
- Revision: r0p1-00rel0
- ARM ETM architecture version 3.5
- Embedded trace buffer (ETB)
- ETB RAM: 1 KB

Data Watchpoint Trace (DWT)
- Use to implement watch points, data tracing and system profiling
- 4 comparators for watchpoints and triggers

CoreSight™ Instrumentation Trace Macrocell (ITM)
- Supports printf style debugging to trace operating systems
- Generates diagnostic system information
**Boundary Scan (7,5,3)**

Provides a serial IO interface for diagnostic and debugging
- Sub-blocks internal to the MCU
- Interconnects external to the MCU
- Infrastructure integrity

Complies with IEEE Standard 1149.1 and IEEE Standard Test Access Port and Boundary-Scan Architecture

JTAG clock speed: up to 25 MHz
Supports various modes
- Bypass, Extest, Sample/Preload, Clamp, High Z, IDCODE

Simplified implementation of boundary scan
Code and Data Flash (7)

On-chip code and data flash for storing user applications and data

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Code Flash</th>
<th>Data Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Size (KB)</td>
<td>4096</td>
<td>64</td>
</tr>
<tr>
<td>Min. Program/Erase Cycles (cycles)</td>
<td>1 K</td>
<td>125 K</td>
</tr>
<tr>
<td>Data Retention Period (years)</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Read Cycles</td>
<td>3 @ 240 MHz</td>
<td>7 @ 60 MHz</td>
</tr>
<tr>
<td>Minimum Prog. Unit (B)</td>
<td>256</td>
<td>4</td>
</tr>
<tr>
<td>Minimum Erasing Unit (KB)</td>
<td>8 or 32</td>
<td>64</td>
</tr>
<tr>
<td>Value After Erase</td>
<td>0xFF</td>
<td>Undefined</td>
</tr>
</tbody>
</table>

Key parameters for on-chip Code and Data Flash

- SCI, SWD, USB, and JTAG
- FACI commands for self-programming
- Security and protection features
  - ID Code for authentication and connection to debugger, etc.
  - Erase/program/read protection

Memory map of a device with 4 MB Code Flash and 64 KB Data Flash
Code and Data Flash (5)

On-chip code and data flash for storing user applications and data

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Code Flash</th>
<th>Data Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Size (KB)</td>
<td>2048</td>
<td>64</td>
</tr>
<tr>
<td>Min. Program/Erase Cycles (cycles)</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td>Data Retention Period (years)</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td>Read Cycles</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td>Minimum Prog. Unit (B)</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td>Minimum Erasing Unit (KB)</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td>Value After Erase</td>
<td>TBD</td>
<td>TBD</td>
</tr>
</tbody>
</table>

Key parameters for on-chip Code and Data Flash

Programming methods
- SCI, SWD, USB, and JTAG
- FACI commands for self-programming

Security and protection features
- ID Code for authentication and connection to debugger, etc.
- Erase/program/read protection

Memory map of a device with 2 MB Code Flash and 64 KB Data Flash
Code and Data Flash (3)

On-chip code and data flash for storing user application and data

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Code Flash</th>
<th>Data Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Size (KB)</td>
<td>1024</td>
<td>16</td>
</tr>
<tr>
<td>Min. Program/Erase Cycles (cycles)</td>
<td>1 K</td>
<td>100 K</td>
</tr>
<tr>
<td>Data Retention Period (years)</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Read Cycles</td>
<td>2 @ 48 MHz</td>
<td>4 @ 48 MHz</td>
</tr>
<tr>
<td>Minimum Prog. Unit (B)</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>Minimum Erasing Unit (KB)</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Value After Erase</td>
<td>0xFF</td>
<td>0xFF</td>
</tr>
</tbody>
</table>

Key parameters for on-chip Code and Data Flash

Programming methods
- SCI, SWD, USB, and JTAG
- FACI commands for self-programming

Security and protection features
- ID Code for authentication and connection to debugger, etc.
- Erase/program/read protection

Memory map of a device with 1 MB Code Flash and 16 KB Data Flash
Code and Data Flash (1)

On-chip code and data flash for storing user application and data

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Code Flash</th>
<th>Data Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Size (KB)</td>
<td>128</td>
<td>4</td>
</tr>
<tr>
<td>Min. Program/Erase Cycles (cycles)</td>
<td>1 K</td>
<td>100 K</td>
</tr>
<tr>
<td>Data Retention Period (years)</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Read Cycles</td>
<td>1 @ 32 MHz</td>
<td>2 @ 32 MHz</td>
</tr>
<tr>
<td>Minimum Prog. Unit (B)</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>Minimum Erasing Unit (KB)</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Value After Erase</td>
<td>0xFF</td>
<td>0xFF</td>
</tr>
</tbody>
</table>

Key parameters for on-chip Code and Data Flash

Programming methods
- SCI and SWD
- FACI commands for self-programming

Security and protection features
- ID Code for authentication and connection to debugger, etc.
- Erase/program/read protection

Memory map of a device with 128 KB Code Flash and 4 KB Data Flash
SRAM (7,5)

On-chip static RAM
Supports no wait read and write access
Up to 640 KB divided in three sections
- SRAM1: 256 KB
- SRAM0: 256 KB (includes 32 KB ECCRAM)
- High Speed RAM: 128 KB
Parity error checking
- A parity bit is added to each word at the time of writing
- Even parity test is performed at the time of reading to detect parity errors
Automatic error checking and correction (ECC) mechanism
- Detects 2-bit errors
- Corrects 1-bit error
NMI generation or reset assertion on error detection
- Parity error
- 1-bit ECC error
- 2-bit ECC error

*No wait states are inserted during reading at up to 200 MHz*
**SRAM (3)**

On-chip static RAM
Supports no wait read and write access
192 divided in two sections
- SRAM1: 64 KB
- SRAM0: 128 KB (includes 16 KB ECCRAM)

Parity error checking
- A parity bit is added to each word at the time of writing
- Even parity test is performed at the time of reading to detect parity errors

Automatic error checking and correction (ECC) mechanism
- Detects 2-bit errors
- Corrects 1-bit error

NMI generation or reset assertion on error detection
- Parity error
- 1-bit ECC error
- 2-bit ECC error

Memory map of a device with 192 KB SRAM
SRAM (1)

On-chip static 16 KB RAM
Supports no wait read and write access
Parity error checking
  ▪ A parity bit is added to each word at the time of writing
  ▪ Even parity test is performed at the time of reading to detect parity errors
**Flash Cache (7,5,3)**

Mechanism to speed up data and instructions read access
Useful at higher system clock frequencies
Frequently used data and instructions are cached in three caches
- 16 B data (operand and DMA) cache
- 32 B instruction pre-fetch cache
- 256 B CPU instruction fetch cache

Flash acceleration is required after 32 MHz and 120 MHz depending on the flash technology.

Simplified implementation of Flash Cache
Memory Protection Units (MPUs) (7,5,3)

Bus-Master MPU
Bus Master MPU monitors the addresses of bus master access to the overall address space
Internal reset or non-maskable interrupts will be generated if access to the protected region is detected
Master groups
- Group A: DMA bus
- Group B: EHER bus*
- Group C: GPX bus*
Number of regions
- Group A: 32 regions**
- Group B: 8 regions*
- Group C: 8 regions*
Setting the address where regions start and end
Setting to make memory protection effective/ineffective in individual regions
Access-control information setting for individual regions
Register can be detected from illegal writing

* Available in S7,S5 series. **S3 series has 16 regions
Memory Protection Units (MPUs) (7,5,3)

Bus-Slave MPU
Bus Slave MPU checks access to bus slave function (for example, Flash, SRAM)
Internal reset or non-maskable interrupts or exception will be generated if access to the protected region is detected
Protect bus master
- Group A: DMA bus
- Group B: EHER bus*
- Group C: GPX bus*
Protect slave function
- Code flash, data flash, SRAM, peripherals, external memory, and external device
Access-control information setting for individual regions
Register can be detected from illegal writing

* Available in S7,S5 series.
Memory Mirror Function (MMF) (7,5,3)

Maps the desired application codebase address in the flash memory to a virtual address in the memory mirror space (8 MB)

Provides mechanism to

- Map load address of multiple application code images to a common virtual address
- Execute multiple versions of the application code in the flash
- User application code
- Resides at different physical addresses in the flash memory
- Is always developed and linked to run from a virtual address
- Requires no context of its physical base address and can be stored into arbitrary flash location at load time
**Ethernet MAC Controller (ETHERC) (7)**

Two integrated Ethernet MACs
IEEE 802.3x-compliant flow control
Provides IEEE 802.3u-compliant Media Independent Interface (MII) and Reduced MII (RMII) for connection with external PHY (optical, twisted wire, etc.) in both ports
10 Mbps or 100 Mbps data transfer rate
Supports IEEE 1588v2 PTP
Dedicated Ethernet DMA controller for data transfer without CPU intervention
Supports full-duplex and half-duplex transfer modes
Supports Magic Packet™ detection and Wake-on-LAN (WOL) functionality
  - Enables remote activation of peripherals
Pause frame flow control
  - Automatic transmission
  - Manual transmission
  - Reception

Connecting an external PHY with the Synergy MCU via MII and RMII interfaces
Ethernet MAC Controller (ETHERC) (5)

Integrated Ethernet MAC
IEEE 802.3x-compliant flow control
Provides IEEE 802.3u-compliant Media Independent Interface (MII) and Reduced MII (RMII) for connection with external PHY (optical, twisted wire, etc.) in both ports
10 Mbps or 100 Mbps data transfer rate
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- Pause frame flow control
- Automatic transmission
- Manual transmission
- Reception

Connecting an external PHY with the Synergy MCU via MII and RMII interfaces
**Ethernet DMA Controller (EDMAC) (7)**

3-channel DMA controller for Ethernet
- 2 channels for Ethernet controllers
- 1 channel for Ethernet PTP controller

Independent TX and RX FIFO per channel enable simultaneous use of multiple channels

Controls TX and RX buffer management for communication to enable efficient data transmission and reception

Uses information (buffer size, address, TX and RX status) in TX and RX descriptor for data transmission and reception

Round-robin channel priority assignment

**Transmission and Reception Modes**
- Single Buffer Per Frame
- Multiple Buffers Per Frame

Simplified implementation of Ethernet DMA Controller
Ethernet DMA Controller (EDMAC) (5)

2-channel DMA controller for Ethernet

- 1 channels for Ethernet controllers
- 1 channel for Ethernet PTP controller

Independent TX and RX FIFO per channel enable simultaneous use of multiple channels

Controls TX and RX buffer management for communication to enable efficient data transmission and reception

Uses information (buffer size, address, TX and RX status) in TX and RX descriptor for data transmission and reception

Round-robin channel priority assignment

Simplified implementation of Ethernet DMA Controller
Ethernet PTP Controller (EPTPC) (7)

 Provides a synchronization clock for decentralized communication networks
 Performs packet analysis and field extraction, and generates PTP packets
 Complies with IEEE 1588-2008 v2 Precision Time Protocol
 Used with Ethernet MAC controller and PTP Ethernet DMA controller

Uses packet filtering by MAC address to separate PTP packets
Supports promiscuous mode
Multiple interrupt sources

Simplified implementation of the Ethernet PTP Controller
Ethernet PTP Controller (EPTPC) (5)

Provides a synchronization clock for decentralized communication networks
Performs packet analysis and field extraction, and generates PTP packets
Complies with IEEE 1588-2008 v2 Precision Time Protocol
Used with Ethernet MAC controller and PTP Ethernet DMA controller

Clock Devices Supported
- End-to-End Transparent Clock
- Peer-to-Peer Transparent Clock
- Ordinary Clock
- Boundary Clock

Uses packet filtering by MAC address to separate PTP packets
Supports promiscuous mode
Multiple interrupt sources

Simplified implementation of the Ethernet PTP Controller
USB 2.0 High-Speed Module (USBHS) (7,5)

Integrated USBHS controller and transceiver
480 Mbps transfer speed
Self-powered and bus-powered operation

Host mode (HS, FS and LS)
- Automatic SOF and packet transmission scheduling
- Programmable intervals for isochronous and interrupt transfers

Device mode (HS and FS)
- Control transfer stage control function
- Device state control function
- SOF interpolation function

Compliant with Battery Charging Class specification Rev 1.2
- Control, bulk, interrupt, isochronous

Integrated buffer memory providing 10 pipes
Flexible endpoint assignment

Simplified block diagram of USB 2.0 High-Speed Module
USB 2.0 Full-Speed Module (USBFS) (7, 5, 3, 1)

Integrated USBFS controller and transceiver
Crystal-less operation*
12 Mbps transfer speed
Self-power and bus-powered operation

** Operation Modes
- Host**
- Device
- On-The-Go**

Host mode
- Automatic SOF and packet transmission scheduling
- Programmable intervals for isochronous and interrupt transfers

Device mode
- Control transfer stage control function
- Device state control function
- SOF interpolation function

Compliant with Battery Charging Class specification Rev 1.2***

Transfer types
- Control, bulk, interrupt, isochronous
Integrated buffer memory providing 10 pipes****
On-chip pull-up and pull-down resistors for D+ and D- signals

* Available in device mode in S1 series only. ** Not available on S1 series. *** Not available on S7, S5 series. **** S1 series has 5 pipes
# Comparison Between USB Modules

<table>
<thead>
<tr>
<th>Features</th>
<th>USB2.0 High-Speed Module</th>
<th>USB2.0 Full-Speed Module</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Host Speed (Mbps)</strong></td>
<td>480, 12, and 1.5</td>
<td>12</td>
</tr>
<tr>
<td><strong>Device Speed (Mbps)</strong></td>
<td>480 and 12</td>
<td>12</td>
</tr>
<tr>
<td><strong>On-The-Go</strong></td>
<td>Available</td>
<td>Available</td>
</tr>
<tr>
<td><strong>Communication Data Transfer Type</strong></td>
<td>Control transfer Bulk transfer Interrupt transfer Isochronous transfer</td>
<td>Control transfer Bulk transfer Interrupt transfer Isochronous transfer</td>
</tr>
<tr>
<td><strong>Buffer Memory (no. of pipes)</strong></td>
<td>10 (includes control pipe)</td>
<td>10 (includes control pipe)</td>
</tr>
<tr>
<td><strong>Battery charging revision 1.2</strong></td>
<td>Available</td>
<td>-</td>
</tr>
<tr>
<td><strong>Clock Recovery</strong></td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>External Power Supply (LDO)</strong></td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td><strong>Internal Registers</strong></td>
<td>D+/D- line, Pull-up/Pull-down</td>
<td>D+/D- line, Pull-up/Pull-down</td>
</tr>
<tr>
<td><strong>Available In</strong></td>
<td><img src="image" alt="S7" /> <img src="image" alt="S5" /></td>
<td><img src="image" alt="S7" /> <img src="image" alt="S5" /></td>
</tr>
</tbody>
</table>
CAN Module

Bus standard for multi-master, message-based protocol
ISO 11898-1, CAN 2.0A, CAN 2.0B compliant
Supports standard (11-bit) and extended ID (29-bit) messaging formats
32 mailboxes, 2 mailbox modes
  ▪ Normal mailbox mode: 32 mailboxes
  ▪ FIFO mailbox mode: 24 mailboxes
Up to 1 Mbps transmission bit rate
8 independent acceptance filters
16-bit time stamping
Error status monitoring
Multiple interrupt sources

Additional Modes
- Sleep
- Listen-only
- Loopback
- External
- Internal

CAN operation using Synergy MCUs
(as a simple communication gateway)
SD/MMC Host Interface (SDHI) (7,5,3)

Provides Secure Digital Host Interface (SDHI) and Multi Media Card (MMC) interface

SDHI
- Supports 1-bit and 4-bit bus
- Supports SD, SDHC, SDXC formats

MMC
- Supports 1-bit, 4-bit and 8-bit MMC bus
- Supports eMMC 4.51 device access
- High speed SDR mode available
- Write protect support
  - Command based
  - Switch based
- Error checking function
  - CRC7 for command and response
  - CRC16 for data
- Card detection support
- Multiple interrupt requests

Simplified block diagram of the SD/MMC Host Interface
Serial Communications Interface (SCI) (7,5,3,1)

Combination of 5 independent asynchronous and synchronous serial interface blocks

- Asynchronous Mode (UART)
  - Receive error and break detection
  - Multi-processor communication function

- Clock Synchronous Mode
  - 8-bit data length only
  - Receive error detection

- Simple IIC Mode
  - Single master only
  - Up to 400 kbps transmission rate

- Simple SPI Mode
  - 8-bit data length only
  - Overrun error detection

- Smart Card Mode
  - ISO/IEC 7816-3
  - Error processing

Bit rate modulation
Integrated noise cancelling
Multiple interrupt sources
Event Link Controller function output

Modes of Operation

Functional block diagram of the Serial Communications Interface
Infrared Data (IrDA) Interface (7,5,3)

Wireless infrared serial communication
IrDA 1.0-compliant encoding and decoding
Up to 115200 bps transmission rate
RX and TX pins multiplexed with SCI
Transfer rate controlled through software

IrDA operation using Synergy MCUs
Quad Serial Peripheral Interface (QSPI) (7,5,3)

4-bit multiplexed serial interface with greater bandwidth over SPI

8-bit, 16-bit, 24-bit, and 32-bit address width
Faster and easier access to external serial flash, EEPROM, FeRAM
- 64-MB external QSPI device space
- Timing adjustment function
- Supports various ROM/flash read instructions
- Direct communication function
- Multiple interrupt sources

Simplified implementation of QSPI
Serial Peripheral Interface (SPI) (7,5,3,1)

Legacy serial communication interface

Configuration
- Multi-master
- Single-master
- Slave
- 3-Wire
- 4-Wire

Modes of operation
- Full-duplex
- Transmit only
- Loopback

Up to 30 Mbps data transmission rate
128-bit RX/TX buffers
Configurable TX word size from 8 to 32 bits

Error detection
- Mode fault
- Overrun
- Parity

Multiple interrupt sources
Event Link Controller function output

Multi-master, multi-slave SPI operation using Synergy MCUs
I2C Bus Interface (IIC) (7,5,3,1)

Multi-master, serial, single-ended bus
Configuration
- Legacy IIC
- System Management Bus (SMBus) v2.0
Modes of operation
- Master TX/RX
- Slave TX/RX
Up to 1 Mbps data transmission rate
7-bit or/and 10-bit address formats
Address match detection
- Slave
- General call
- Device ID
- SMBus host address
Integrated noise cancelling
Automatic clock low-hold
Bus hanging timeout
Multiple interrupt sources
Event Link Controller function output

IIC operation using Synergy MCUs
Serial Sound Interface (SSI) (7,5,3)

Serial interface to transfer PCM/audio data
Supports non-compressed serial audio streams
- Slave receiver
- Slave transmitter
- Slave transceiver
- Master receiver
- Master transmitter
- Master transceiver
Clock master and slave modes
1 MHz to 50 MHz oversampling clock
Includes 8-stage FIFO buffers in TX and TR
Supports interrupt and DMA driven data reception and transmission

SSI operation using Synergy MCUs
Sampling Rate Converter (SRC) (7,5)

Converts the sampling rate of data produced by various decoders (for example, WMA, MP3, or AAC)
16-bit data size for stereo and monaural data
Independent input and output FIFOs
Selectable sampling rate:

Processing capacity: 7.7 µs (max) sample output interval
80 dB SNR
Two DMA transfer sources
Multiple interrupt sources
External Memory Bus (7,5,3)

Allows MCU bus master access to external slave memories and peripherals
Arbitrates requests for bus mastership on external address space and external bus control registers on the CPU bus and other bus masters
Up to 120 MHz external bus speed
Supports division of external address space into 8 CS areas and an SDRAM area

CS area controller
- Configurable bus width, 8 or 16 bits
- Up to 15 cycles for read and write recovery
- CS area up to 16 MB

SDRAM area controller
- Up to 120 MHz burst transfers
- Self-refresh and auto-refresh selection
- SDRAM area up to 64 MB

Interfacing an external memory with the Synergy MCU using the External Memory Bus
Analog

12-Bit A/D Converter
14-Bit A/D Converter
12-Bit D/A Converter
Low-Power Analog Comparator
High-Speed Analog Comparator
PGA
OPAMP
Temperature Sensor*
14-Bit A/D Converter (ADC14) (1,3)

14-bit resolution, 1.4-Msps, SAR ADC

Inputs
- Up to 28 external multiplexed analog input channels
- Internal temperature sensor
- Internal reference voltage

Multiple trigger sources
- Internal: ELC (PWM, timer, etc.)
- External: (via ELC)

Built-in ADC Diagnostics
- Hardware averaging/oversampling
- Multiple interrupt sources
- Event Link Controller function output

Simplified block diagram of the 14-Bit A/D Converter
12-Bit A/D Converter (ADC12) (7,5)

23 (max.) external analog input channels
12-bit resolution, 2.5-MSPS, SAR ADC

Inputs
- Multiplexed analog input channels
- Internal temperature sensor
- Internal reference voltage

Multiple trigger sources
- Internal: ELC (PWM, timer, etc.)
- External: (via ELC)

Built-in ADC Diagnostics
- Hardware averaging/oversampling
- Multiple interrupt sources
- Event Link Controller function output

Sampling Modes
- **Single Scan**
  - AD conversion is performed only once on the input channels
- **Continuous Scan**
  - AD conversion is performed continuously on the input channels
- **Group Scan**
  - AD conversion is performed one by one only on the input channels in the group

Simplified block diagram of the 12-Bit A/D Converter
## Comparison Between A/D Converters (7,3,5,1)

<table>
<thead>
<tr>
<th>Features</th>
<th>14-Bit A/D Converter</th>
<th>12-Bit A/D Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. No. of Input Channels</td>
<td>28</td>
<td>18</td>
</tr>
<tr>
<td>A/D Conversion Method</td>
<td>Successive approximation method</td>
<td>Successive approximation method</td>
</tr>
<tr>
<td>Resolution (bits)</td>
<td>14 (default)</td>
<td>12 (default)</td>
</tr>
<tr>
<td></td>
<td>Can be selected between 12 and 14</td>
<td>Can be selected between 8, 10, and 12</td>
</tr>
<tr>
<td>Conversion Time (μs/ channel)</td>
<td>0.7</td>
<td>0.4</td>
</tr>
<tr>
<td>Maximum A/D Conversion Clock (MHz)</td>
<td>PCLKB = 48 PCLKC = 64</td>
<td>PCLKB = 32 PCLKC = 64</td>
</tr>
<tr>
<td></td>
<td>PCLKB = 60 PCLKC = 60</td>
<td>TBD</td>
</tr>
<tr>
<td>Modes of Operation</td>
<td>Single scan mode</td>
<td>Single scan mode</td>
</tr>
<tr>
<td></td>
<td>Continuous scan mode</td>
<td>Continuous scan mode</td>
</tr>
<tr>
<td></td>
<td>Group scan mode</td>
<td>Group scan mode</td>
</tr>
<tr>
<td>A/D Conversion Start Triggers</td>
<td>Software trigger</td>
<td>Software trigger</td>
</tr>
<tr>
<td></td>
<td>Asynchronous trigger</td>
<td>Asynchronous trigger</td>
</tr>
<tr>
<td></td>
<td>From Event Link Controller</td>
<td>From Event Link Controller</td>
</tr>
<tr>
<td>Channel-Dedicated Sample and Hold Circuit</td>
<td>-</td>
<td>Available</td>
</tr>
<tr>
<td>Programmable Gain Amplifier</td>
<td>-</td>
<td>Available</td>
</tr>
<tr>
<td>ADC Diagnostics</td>
<td>Available</td>
<td>Available</td>
</tr>
<tr>
<td>Available in</td>
<td>S3</td>
<td>S1</td>
</tr>
<tr>
<td></td>
<td>S7</td>
<td>S5</td>
</tr>
</tbody>
</table>

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12-Bit D/A Converter (DAC12) (7,5,3,1)

12-bit resolution
Integrated output amplifier
Reference voltage inputs
- Internal
- External
16-bit R/W data registers
Can be operated in-sync or out-of-sync with ADC
Output retention in low power modes
Event Link Controller function output
High-Speed Analog Comparator (ACMPHS) (7,5)

Compares a test voltage with a reference voltage and provides a digital output

Analog input voltage
- Output of DAC, input from ADC, output of PGA*, and internal VREF**

Reference voltage
- Output of DAC, input from ADC, and internal VREF

Integrated noise filter
- Selectable sampling frequency

Multiple interrupt sources
Event Link Controller function output

* Available on S7,S5 series only. ** Available on S3 series only
Low-Power Analog Comparator (ACMPLP) (1,3)

Compares a test voltage with a reference voltage and provides a digital output

- Analog input voltage
  - Input from CMPIN pin
- Reference voltage
  - Input from CMPREF pin, Internal reference voltage
- Integrated noise filter
- Selectable sampling frequency
- Multiple interrupt sources
- Event Link Controller function output

Simplified block diagram of the Low-Power Analog Comparator
Comparison Between Analog Comparators

<table>
<thead>
<tr>
<th>Features</th>
<th>High-Speed Analog Comparator</th>
<th>Low-Power Analog Comparator</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Channels</td>
<td>6</td>
<td>TBD</td>
</tr>
<tr>
<td><strong>Analog Input Voltage</strong></td>
<td>Output of internal PGA</td>
<td>Output of internal D/A converter</td>
</tr>
<tr>
<td></td>
<td>Output of internal D/A converter</td>
<td>Input of internal A/D converter</td>
</tr>
<tr>
<td></td>
<td>Input of internal A/D converter</td>
<td>Internal reference voltage (Vref)</td>
</tr>
<tr>
<td><strong>Reference Voltage</strong></td>
<td>Internal reference voltage (Vref)</td>
<td>Output from internal D/A converter</td>
</tr>
<tr>
<td></td>
<td>Output from internal D/A converter</td>
<td>Input from internal A/D converter</td>
</tr>
<tr>
<td></td>
<td>Input from internal A/D converter</td>
<td>Internal reference voltage (Vref)</td>
</tr>
<tr>
<td>Window Mode</td>
<td>-</td>
<td>Available</td>
</tr>
<tr>
<td>Event Link Output</td>
<td>Available</td>
<td>Available</td>
</tr>
<tr>
<td>Output Delay Time (ns)</td>
<td>50</td>
<td>5000*</td>
</tr>
<tr>
<td>Operating Current (μA)</td>
<td>70</td>
<td>2*</td>
</tr>
</tbody>
</table>

Available In

*At low speed mode*
Programmable Gain Amplifier (PGA) (7,5)

Integrated programmable gain amplifier with differential inputs
Amplifies analog input signals to enable conversions using the ADC
Biases differential input signals with the reference voltage generated by the on-chip DAC and then amplifies them
- Selectable bias voltage (AVCC*0.5 or AVCC*0.6)

Gain error = 1 @ gain 4.00
Offset error = 8 mV
Useful in data acquisition, signal conditioning, and instrumentation applications

Simplified implementation of Programmable Gain Amplifier
Operational Amplifier (OPAMP) (1,3)

Integrated small signal operational amplifier with a differential input pair
Op-amp's output can be used as input to the analog comparator or the ADC
Supports high-speed and low-speed operation
Activated by the asynchronous timer and de-activated by the ADC conversion end trigger
Temperature Sensor (7,5)

Outputs a voltage directly proportional to the die temperature
Used to determine and monitor die temperature for reliable operation of the device
The output voltage is provided to the ADC
±1°C accuracy over the operating range
4.1 mV/°C temperature gradient
Fairly linear relationship between the die temperature and output voltage

Temperature Determination

Slope Method
✓ Use pre-calculated temperature gradient.
✓ \( t = (v - 1157.5) / 4.1 \)
where
\( t \): predicted die temperature,
\( v \): output voltage of temperature sensor.

Two Point Method
✓ Calculate temperature gradient for your device to eliminate error due to variation induced from device to device.
✓ \( m = (v_2 - v_1) / (t_2 - t_1) \)
✓ \( t = (v - 1157.5) / m \)
where
\( (v_1, t_1) \) and \( (v_2, t_2) \): voltage and temperature measured at two experimental points,
\( m \): calculated temperature gradient,
\( t \): predicted die temperature,
\( v \): output voltage of temperature sensor.

Simplified block diagram and characteristics of the Temperature Sensor
Temperature Sensor (1,3)

Outputs a voltage inversely proportional to the die temperature
Used to determine and monitor die temperature for reliable operation of the device
The output voltage is provided to the ADC
±1°C accuracy over operating range
-3.65 mV/°C temperature gradient
Fairly linear relationship between the die temperature and the output voltage

**Temperature Determination**

- **Two Point Method**
  - Calculate temperature gradient for your device to eliminate error due to variation induced from device to device.
  - Use pre-calculated temperature gradient.
  - \( t = \frac{(1141.25 - v)}{m} \)
  - \( m = \frac{(v_2 - v_1)}{t_2 - t_1} \)
  - \( t = \frac{(1141.25 - v)}{m} \)
  - where
  - \((v_1, t_1)\) and \((v_2, t_2)\): voltage and temperature measured at two experimental points,
  - \(m\): calculated temperature gradient,
  - \(t\): predicted die temperature,
  - \(v\): output voltage of temperature sensor.

- **Slope Method**
  - Use pre-calculated temperature gradient.
  - \( t = \frac{(1141.25 - v)}{3.65} \)
  - where
  - \(t\): predicted die temperature,
  - \(v\): output voltage of temperature sensor.

Simplified block diagram and characteristics of the Temperature Sensor
SysTick (7,5,3,1)

24-bit, decrementing, clear-on-write, reload-on-zero timer
Integrated into the NVIC

Clock source
- Processor’s clock from main oscillator
- Low-Speed On-Chip Oscillator (32.788 kHz)

Flexible control mechanism
Use for
- System heartbeat for RTOS
- System task-scheduling using a periodic SysTick interrupt
- Dynamic clock management
- Real-time interval measurement
- Typical counter/general timer

Simplified implementation of SysTick timer
Clock Management (7)

Multiple clock sources enable flexible operation and optimization of devices across a variety of power and performance points.

<table>
<thead>
<tr>
<th>Clock Generation Sources</th>
<th>Details</th>
</tr>
</thead>
</table>
| Main Clock Oscillator    | ✓ 8 to 24 MHz resonator frequency  
                          | ✓ Up to 24 MHz external clock frequency  
                          | ✓ Drive capability switching  
                          | ✓ Automatic clock switching upon oscillation stop detection |
| Sub-Clock Oscillator     | ✓ Requires 32.768 kHz external crystal  
                          | ✓ Drive capability switching |
| PLL                      | ✓ 8 to 24 MHz input frequency  
                          | ✓ 120 to 240 MHz output frequency |
| On-Chip Oscillator       | ✓ High-speed: 16, 18, 20 MHz  
                          | ✓ Middle-speed: 8 MHz  
                          | ✓ Low-speed: 32.768 kHz |
| Independent Watchdog Timer Oscillator | ✓ Dedicated for watchdog timer operation  
                          | ✓ 15 kHz |
| External Debugging Clock | ✓ For JTAG, SWD  
                          | ✓ Up to 25 MHz |

Clock distribution tree in the Synergy MCU

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Clock Management (5)

Multiple clock sources enable flexible operation and optimization of devices across a variety of power and performance points.

### Main Clock Oscillator
- 8 to 24 MHz resonator frequency
- Up to 24 MHz external clock frequency
- Drive capability switching
- Automatic clock switching upon oscillation stop detection

### Sub-Clock Oscillator
- Requires 32.768 kHz external crystal
- Drive capability switching

### PLL
- 8 to 24 MHz input frequency

### On-Chip Oscillator
- High-speed: 16, 18, 20 MHz
- Middle-speed: 8 MHz
- Low-speed: 32.768 kHz

### Independent Watchdog Timer Oscillator
- Dedicated for watchdog timer operation
- 15 kHz

### External Debugging Clock
- For JTAG, SWD
- Up to 25 MHz

---

Clock distribution tree in the Synergy MCU

---
Clock Management (3)

Multiple clock sources enable flexible operation and optimization of devices across a variety of power and performance points.

- **Main Clock Oscillator**
  - 1 to 20 MHz resonator frequency
  - Up to 20 MHz external clock frequency
  - Drive capability switching
  - Automatic clock switching upon oscillation stop detection

- **Sub-Clock Oscillator**
  - Requires 32.768 kHz external crystal
  - Drive capability switching

- **PLL**
  - 4 to 12.5 MHz input frequency
  - 24 to 64 MHz output frequency

- **On-Chip Oscillator**
  - High-speed: 24, 32, 48, 64 MHz
  - Middle-speed: 8 MHz
  - Low-speed: 32.768 kHz

- **Independent Watchdog Timer Oscillator**
  - Dedicated for watchdog timer operation
  - 15 kHz

- **External Debugging Clock**
  - For JTAG, SWD
  - Up to 25 MHz
Clock Management (1)

Multiple clock sources enable flexible operation and optimization of devices across a variety of power and performance points

Clock Generation Sources

- **Main Clock Oscillator**
  - 1 to 20 MHz resonator frequency
  - Up to 20 MHz external clock frequency
  - Drive capability switching
  - Automatic clock switching upon oscillation stop detection

- **Sub-Clock Oscillator**
  - Requires 32.768 kHz external crystal
  - Drive capability switching

- **On-Chip Oscillator**
  - High-speed: 24, 32, 48, 64 MHz
  - Middle-speed: 8 MHz
  - Low-speed: 32.768 kHz

- **Independent Watchdog Timer Oscillator**
  - Dedicated for watchdog timer operation
  - 15 kHz

- **External Debugging Clock**
  - For SWD
  - Up to 25 MHz

Clock distribution tree in the Synergy MCU

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Data Transfer Controller (DTC) (7,5,3,1)

Transfers data between memory and peripherals without CPU intervention. DTC is activated by peripheral interrupts.

**Modes of Transfer**

- **Normal Transfer Mode**
  - One data transfer per activation

- **Repeat Transfer Mode**
  - One data transfer per transfer request
  - Max. no. of repeat t/f: 256
  - Max. t/f data size = 256 x 32 bit = 1 KB

- **Block Transfer Mode**
  - One block data transfer per activation
  - Max. block size = 1 KB

Data transfer unit size: 1 byte (8 bits), 1 word (16 bits), 1 longword (32 bits)

1 to 256 data units (word) per block

Supports chained transfers and sophisticated data scatter/gathering

Interrupt generation upon transfer completion

Event Link Controller function output

Simplified implementation of the Data Transfer Controller
DMA Controller (DMAC) (7,5,3,1)

Allows data transfer without CPU intervention
Up to 8 independent channels with pre-assigned priority
8, 16, and 32 bits per word
Maximum 64 M words per data transfer

Modes of Transfer

- **Normal Transfer Mode**
  - One data transfer per activation
  - Free running mode supported

- **Repeat Transfer Mode**
  - One data transfer per transfer request
  - Repeat size: 1024 (1 K words)

- **Block Transfer Mode**
  - One block data transfer per activation
  - Max. block capacity = 1024 (1 K words)
  - Max. block transfer = 64 K blocks (that is 64 M words)

Multiple interrupt outputs to CPU or DTC upon transfer completion
Interrupt generation upon completion of transfer

Simplified implementation of the DMA Controller
Event Link Controller (ELC) (7,5,3,1)

Allows direct interaction between different modules without CPU intervention
Routes source events generated by a peripheral to event inputs on other peripherals
Event signal can activate a peripheral for the desired operation
- Start/stop/clear timer, up/down counting
- Start ADC and DAC conversion
- Start cap touch measurement
- Start DMA/DTC transfer
- Issue interrupts to the CPU
- Change state of GPIOs
Most peripherals generate event signals

Peripheral classification based on event signals

<table>
<thead>
<tr>
<th>Peripherals</th>
<th>Event Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>Only Generate Event Signals</td>
<td></td>
</tr>
<tr>
<td>Only Accept Event Signals</td>
<td></td>
</tr>
<tr>
<td>Generate and Accept Event Signals</td>
<td></td>
</tr>
</tbody>
</table>

Simplified implementation of the Event Link Controller
Low Power Modes (7,5,3,1)

Low power modes provide operational flexibility which can dramatically reduce current consumption. Independent wake-up signals for data acquisition and data transmission peripherals. Allow operation of a peripheral while keeping the CPU and other peripherals disabled. Data and state retention.

<table>
<thead>
<tr>
<th>Mode of Operation</th>
<th>Core</th>
<th>Flash</th>
<th>SRAM</th>
<th>RTC, AGT, Vbatt, LVD</th>
<th>Other Peripherals</th>
<th>IO Pins</th>
<th>Snooze</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>Operating</td>
<td>Selectable</td>
<td>Selectable</td>
<td>Selectable</td>
<td>Selectable</td>
<td>Selectable</td>
<td>NA</td>
</tr>
<tr>
<td>Sleep</td>
<td>Clock Gated</td>
<td>Selectable</td>
<td>Selectable</td>
<td>Selectable</td>
<td>Selectable</td>
<td>Selectable</td>
<td>NA</td>
</tr>
<tr>
<td>Software Standby</td>
<td>Clock Gated</td>
<td>Data Retained</td>
<td>Data Retained</td>
<td>Selectable</td>
<td>State Retained</td>
<td>State Retained</td>
<td>Available</td>
</tr>
<tr>
<td>Deep Software Standby</td>
<td>Powered Off</td>
<td>Powered Off</td>
<td>Powered Off</td>
<td>Selectable</td>
<td>Powered Off</td>
<td>State Retained</td>
<td>NA</td>
</tr>
</tbody>
</table>

Comparison among various modes of operation

<table>
<thead>
<tr>
<th>Mode of Operation</th>
<th>S7</th>
<th>S5</th>
<th>S3</th>
<th>S1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal (mA)</td>
<td>41</td>
<td>TBD</td>
<td>15.8</td>
<td>3.8</td>
</tr>
<tr>
<td>Sleep (mA)</td>
<td>23</td>
<td>TBD</td>
<td>6.8</td>
<td>1.9</td>
</tr>
<tr>
<td>Software Standby (μA)</td>
<td>2000</td>
<td>TBD</td>
<td>1.7</td>
<td>0.8</td>
</tr>
<tr>
<td>Deep Software Standby (μA)</td>
<td>4.5</td>
<td>TBD</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Typical current consumption in various modes of operation (target values)
Low Power Modes (7)

<table>
<thead>
<tr>
<th>Mode of Operation →</th>
<th>Normal</th>
<th>Sleep</th>
<th>Software Standby</th>
<th>Deep Software Standby</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Test Conditions ↓</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Consumption (mA)</td>
<td>41</td>
<td>23</td>
<td>2</td>
<td>0.0045</td>
</tr>
<tr>
<td>$V_{CC}$ (V)</td>
<td>3.3</td>
<td>3.3</td>
<td>3.3</td>
<td>3.3</td>
</tr>
<tr>
<td>$V_{batt}$ (V)</td>
<td>3.3</td>
<td>3.3</td>
<td>3.3</td>
<td>3.3</td>
</tr>
<tr>
<td>System Frequency (MHz)</td>
<td>240</td>
<td>240</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Code</td>
<td>While (1)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Systems State</th>
<th>CPU</th>
<th>Flash</th>
<th>SRAM</th>
<th>RTC, LVD, OSC</th>
<th>Other Peripherals</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating</td>
<td>Clock Gated</td>
<td>Selectable</td>
<td>Selectable</td>
<td>Selectable</td>
<td>Disabled</td>
</tr>
<tr>
<td>Clock Gated</td>
<td>Clock Gated</td>
<td>Data Retained</td>
<td>Data Retained</td>
<td>Data Retained</td>
<td>Disabled</td>
</tr>
<tr>
<td>Power Off</td>
<td>Selectable</td>
<td>Data Retained</td>
<td>Data Retained</td>
<td>Disabled</td>
<td>Power Off</td>
</tr>
</tbody>
</table>

Current consumption (target, typical) and test conditions for various modes of operation

*ICLK=60 MHz
** wake up by MOCO

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### Low Power Modes (5)

<table>
<thead>
<tr>
<th>Mode of Operation →</th>
<th>Normal</th>
<th>Sleep</th>
<th>Software Standby</th>
<th>Deep Software Standby</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Test Conditions ↓</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Consumption (mA)</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td>$V_{CC}$ (V)</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td>Vbatt (V)</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
<tr>
<td>System Frequency (MHz)</td>
<td>TBD</td>
<td>TBD</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Code</td>
<td>While (1)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

#### Systems State

- **CPU**: Operating → Clock Gated → Clock Gated → Power Off
- **Flash**: Selectable → Selectable → Data Retained → Power Off
- **SRAM**: Selectable → Selectable → Data Retained → Power Off
- **RTC, LVD, OSC**: Selectable → Selectable → Disabled → Disabled
- **Other Peripherals**: Disabled → Disabled → Retained → Power Off

Current consumption (target, typical) and test conditions for various modes of operation.
### Low Power Modes (3)

<table>
<thead>
<tr>
<th>Mode of Operation →</th>
<th>Normal</th>
<th>Sleep</th>
<th>Software Standby</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Test Conditions ↓</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Consumption (mA)</td>
<td>15.8</td>
<td>6.8</td>
<td>0.0017</td>
</tr>
<tr>
<td>VCC (V)</td>
<td>3.3</td>
<td>3.3</td>
<td>3.3</td>
</tr>
<tr>
<td>Vbatt (V)</td>
<td>3.3</td>
<td>3.3</td>
<td>3.3</td>
</tr>
<tr>
<td>System Frequency (MHz)</td>
<td>48</td>
<td>48</td>
<td>NA</td>
</tr>
<tr>
<td>Code</td>
<td>While (1)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

#### Systems State

<table>
<thead>
<tr>
<th>Component</th>
<th>Normal</th>
<th>Sleep</th>
<th>Software Standby</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>Operating</td>
<td>Clock Gated</td>
<td>Clock Gated</td>
</tr>
<tr>
<td>Flash</td>
<td>Selectable</td>
<td>Data Retained</td>
<td>Data Retained</td>
</tr>
<tr>
<td>SRAM</td>
<td>Data Retained</td>
<td>Data Retained</td>
<td>Data Retained</td>
</tr>
<tr>
<td>RTC, LVD, OSC</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Selectable</td>
</tr>
<tr>
<td>Other Peripherals</td>
<td>Disabled</td>
<td>Disabled</td>
<td>Retained</td>
</tr>
</tbody>
</table>

Current consumption (target, typical) and test conditions for various modes of operation.

*ICLK=32 MHz

** wake up by MOCO

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### Low Power Modes (1)

<table>
<thead>
<tr>
<th>Mode of Operation</th>
<th>Normal</th>
<th>Sleep</th>
<th>Software Standby</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Test Conditions</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Consumption (mA)</td>
<td>3.8</td>
<td>1.9</td>
<td>0.0008</td>
</tr>
<tr>
<td>$V_{CC}$ (V)</td>
<td>3.3</td>
<td>3.3</td>
<td>3.3</td>
</tr>
<tr>
<td>$V_{batt}$ (V)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>System Frequency (MHz)</td>
<td>32</td>
<td>32</td>
<td>NA</td>
</tr>
<tr>
<td>Code</td>
<td>While (1)</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

#### Systems State

- **CPU**: Operating → Clock Gated → Clock Gated
- **Flash**: Selectable → Data Retained → Data Retained
- **SRAM**: Data Retained → Data Retained → Data Retained
- **RTC, LVD, OSC**: Disabled → Disabled → Selectable
- **Other Peripherals**: Disabled → Disabled → Retained

*Current consumption (target, typical) and test conditions for various modes of operation*

- In Bus 7 state, $I_{CC}=2.46$ mA @ 32 MHz, 77 $\mu$A/MHz

**Throughput**

- Normal (3.8 mA)
- Sleep (1.9 mA)
- Snooze (Software Standby, 0.8 $\mu$A)

**Power Consumption**

- 5.5 $\mu$s**
- 0.38 $\mu$s*

*ICLK=32 MHz

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Port Function Select (PFS) (7,5,3,1)

Controls routing and assignment of multiple digital signals from different peripherals to different IO pins

Most pins* are multiplexed among different peripherals; that is, many peripherals have their signals mapped to different pin groups

Provides design flexibility to help simplify PCB layout and routing to optimize system performance

Can enable easier migration to different MCU products within the same product family.

* Except power, clock, and analog signals

** Conceptual demonstration only. Please refer to the product documentation for exact pin multiplexing.
Realtime Clock (RTC) (7,5,3,1)

Integrated RTC with calendar functionality
Operates using a 128 Hz clock from either
- Sub-Clock Oscillator, or
- Low-Speed On-Chip Oscillator (LOCO)

Clock error correction function
1 or 64 Hz clock output via RTCOUT pin
Time (year, month, day, date, hour, minute and second) capture upon activity on RTC input pins
Send event signals to other peripherals while CPU is in sleep mode
Interrupt on alarm, periodic interrupt, and several other interrupts

Simplified block diagram of the RTC
Switching Regulator (7)

Integrated DC-DC buck converter for high-efficiency operation (~ typ. 80% at 100 mA)
Reduces power dissipation in the die
Internal digital power rail selection
- Switching Regulator
- LDO Linear Regulator

I\text{Load} = 200 \text{ mA} (\text{typ., in PWM mode})

f\text{Switching} = 1 \text{ MHz} (\text{typ., in PWM mode})

I\text{Quiescent} = 100 \mu\text{A} (\text{typ., in PFM mode})
General PWM Timer 32-Bit Enhanced High Resolution (GPT32EH) (7,5)

32-bit high-resolution timers with PWM
- Up to 4 independent timers 8.3 ns (minimum) resolution
- Capable of adjusting the duty cycle of PWM output in increments of 260 ps delay*

Independent clock selection per timer
2 input/output pins per timer

3-phase PWM generator for high-speed, brushless DC motor control function
- Register write protection
- Output pins disable control
- Ability to trigger ADC conversion
- Multiple interrupt sources
- Data transfer controller (DTC) and DMA activation by all interrupts

Inputs to/outputs from ELC

Modes of Operation, Comparison Table

* Only available when used with Picosecond Delay function
General PWM Timer 32-Bit Enhanced (GPT32E) (7,5)

32-bit high-resolution timers with PWM
- Up to 4 independent timers 8.3 ns (minimum) resolution
- Independent clock selection per timer
- 2 input/output pins per timer

- 3-phase PWM generator for high-speed, brushless DC motor control function
- Protection features
  - Register write protection
  - Output pins disable control
- Ability to trigger ADC conversion
- Multiple interrupt sources
  - Data transfer controller (DTC) and DMA activation by all interrupts
- Inputs to/outputs from ELC

Modes of Operation, Comparison Table

Simplified implementation of
General PWM Timer 32-Bit Enhanced
General PWM Timer 32-Bit (GPT32) (7,5,3,1)

A simplified derivative of 32-bit high-resolution timers
Independent clock selection per timer
2 input/output pins per timer

Inputs
- Input
  - 4 external pin triggers
  - 8 ELC events

Input Event Actions
- Counter start, counter stop, counter clear, count up and count down

Up to 10 independent timers
Automatic dead time insertion (no dead time buffer)
PWM generator for brushless DC motor control function
Protection features
- Register write protection
- Multiple interrupt sources
- Data transfer controller activation and DMA (S3) by all interrupts
Inputs to/outputs from ELC

Modes of Operation, Comparison Table
General PWM Timer 16-Bit (GPT16) (1)

A simplified 16-bit timer
Independent clock selection per timer
2 input/output pins per timer

- Input:
  - 4 external pin triggers
  - 8 ELC events

- Input Event Actions:
  - Counter start, counter stop, counter clear, count up and count down

Up to 6 independent timers
Automatic dead time insertion (no dead time buffer)
PWM generator for brushless DC motor control function
Protection features
  - Register write protection
  - Multiple interrupt sources
  - Data transfer controller activation by all interrupts

Inputs to/outputs from ELC

Modes of Operation, Comparison Table

Simplified implementation of General PWM Timer 16-Bit
# GPTx Modes of Operation (7,3,5,1)

GPT32-EH, GPT32-E, GPT32, and GPT16

<table>
<thead>
<tr>
<th>Modes</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Counter</td>
<td>1. <strong>Periodic count (up and down)</strong>: Up-counting and down-counting is performed by an internal clock. Up-counting is resumed upon overflow. Down-counting is resumed upon underflow.</td>
</tr>
<tr>
<td></td>
<td>2. <strong>Event count (up and down)</strong>: Up-counting and down-counting is performed by an external counting source. Up-counting is resumed upon overflow. Down-counting is resumed upon underflow.</td>
</tr>
<tr>
<td>2. Waveform output by compare match</td>
<td>1. <strong>Low and high</strong>: Timer outputs can be asserted low or high upon match comparison.</td>
</tr>
<tr>
<td></td>
<td>2. <strong>Toggle</strong>: Timer outputs can be asserted low or high upon count match.</td>
</tr>
<tr>
<td>3. Input capture</td>
<td>Timer count value can be captured in registers upon detection of signals on external pins on both the rising edge and the falling edge of the count clock.</td>
</tr>
<tr>
<td>4. Phase counting</td>
<td>The phase difference between a timer’s two input pins is detected and used to determine the counting direction.</td>
</tr>
<tr>
<td>5. PWM</td>
<td>**Automatic dead-time insertion</td>
</tr>
<tr>
<td></td>
<td>1. <strong>Sawtooth wave PWM</strong>: The PWM is generated with a saw tooth wave, and the duty cycle is set by a match value in the register.</td>
</tr>
<tr>
<td></td>
<td>2. <strong>Sawtooth wave one shot</strong>: The PWM is generated with a saw tooth wave, and the pulse width is set by two match values.</td>
</tr>
<tr>
<td></td>
<td>3. <strong>Triangular 1, 2, 3</strong>: The PWM is generated with a triangular wave, and the pulse width is set by two match values at crests or troughs.</td>
</tr>
</tbody>
</table>
## Comparison Between GPTs

<table>
<thead>
<tr>
<th>Features</th>
<th>GPT32-EH</th>
<th>GPT32-E</th>
<th>GPT32</th>
<th>GPT16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Counter Bits</td>
<td>32</td>
<td>32</td>
<td>32</td>
<td>16</td>
</tr>
<tr>
<td>Clocks</td>
<td>PCLK (/4, /16, /64, /256, /1024)</td>
<td>PCLK (/4, /16, /64, /256, /1024)</td>
<td>PCLK (/4, /16, /64, /256, /1024)</td>
<td>PCLK (/4, /16, /64, /256, /1024)</td>
</tr>
<tr>
<td>Counting Mode</td>
<td>Up, Down</td>
<td>Up, Down</td>
<td>Up, Down</td>
<td>Up, Down</td>
</tr>
<tr>
<td>Max. No. of Units</td>
<td>4</td>
<td>4</td>
<td>10</td>
<td>6</td>
</tr>
<tr>
<td>Input Capture</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
</tr>
<tr>
<td>Compare Match Output</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
</tr>
<tr>
<td>ADC Start Request</td>
<td>Available</td>
<td>Available</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Interrupt Sources</td>
<td>13</td>
<td>TBD</td>
<td>13</td>
<td>TBD</td>
</tr>
<tr>
<td>Interrupt Skipping</td>
<td>Available</td>
<td>Available</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>3-Phase PWM Generator</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
<td>Available</td>
</tr>
<tr>
<td>Pico Second Delay</td>
<td>Available</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Available In</td>
<td>S7</td>
<td>S5</td>
<td>S7</td>
<td>S7</td>
</tr>
</tbody>
</table>
Asynchronous General Purpose Timer (AGT) (7,5,3,1)

16-bit asynchronous timer for pulse output, external pulse width (period) measurement, and external event counting

Modes of operation

- **Timer mode**
  - Count source is counted

- **Pulse Output mode**
  - Count source is counted and output is inverted upon timer underflow

- **Event Counter mode**
  - An external event is counted

- **Pulse Width Measurement mode**
  - An external pulse width is measured

- **Pulse Period Measurement mode**
  - An external pulse period is measured

Multiple clock sources

- Peripheral clock (PCLK)
- Low-Speed On-Chip Oscillator (LOCO)
- Sub-clock (fSUB)
- Underflow signal of timer

Can be operated asynchronously in low power mode without the PCLK

Simplified implementation of Asynchronous General Purpose Timer
Watchdog Timer (WDT) (7,5,3,1)

14-bit down-counter, window watchdog timer
Operates using peripheral clock

Start Conditions

- **Auto-Start Mode**
  Counting automatically starts after a reset or underflow or refresh error

- **Register-Start Mode**
  Counting starts by refreshing the counter in the register

Stop Conditions

- **Reset**
  Down-counter and other registers return to their initial values

- **Underflow or Refresh Error**
  Counter underflows or a refresh error is generated

Issues reset on down-counter underflow and refresh error OR
Generates interrupt on down-counter underflow and refresh error
HMI

Capacitive Touch
Sensing Unit
Graphics LCD Controller
Segment LCD Controller
2D Drawing Engine
JPEG Codec
Parallel Data Capture
Capacitive Touch Sensing Unit (CTSU) (7,5,3,1)

Capacitive Touch Sensing Unit allows detection of touch by measuring the change in parasitic electrostatic capacitance of the sensing electrode. Low pass filter input Measurement triggered by software or the Event Link Controller.

Measurement Methods and Modes

- **Self-Capacitance Method**
  - Single-Scan Mode
  Electrostatic capacitance between finger and a single electrode is measured per channel.
  - Multi-Scan Mode
  Electrostatic capacitance between finger and a single electrode is measured per channel successively.

- **Mutual-Capacitance Method**
  - Full-Scan Mode
  Channel capacitance is measured successively by using mutual-capacitance method for higher sensitivity.

Simplified block diagram of Capacitive Touch Sensing Unit
Graphics LCD Controller (GLCDC) (7,5)

Highly configurable peripheral to drive a variety of TFT LCDs; useful for HMI applications
Supports various types of data formats
- 32-bpp formats: αRGB:8888, αRGB:0888
- 16-bpp formats: αRGB:4444, αRGB:1555, αRGB:0565
- Look-up table formats: CLUT8, CLUT4, CLUT1
Layer blending control
- Superimposition of multiple graphic layers
- Display plane selection
- RGB index chroma key
- Alpha blending
Output control
- Dither correction
- Brightness/contrast correction
- Gamma correction
- Flexible generation of external timing control signals (TCON 0123)
Supports digital interface signal output for video image size of WVGA or greater*
- Up to 1024 horizontal lines, 16-line resolution
- Up to 1024 vertical lines, 16-line resolution
Pixel clock source: external clock or internal clock

*Simplified implementation of Graphics LCD Controller

*with limited functionality
### Graphics LCD Controller (7,5)

<table>
<thead>
<tr>
<th>Resolution (pixels)</th>
<th>Layers</th>
<th>Refresh Rate (Hz)</th>
<th>Color Depth (bits per pixel)</th>
<th>Dynamic Graphics Manipulation (Animation)</th>
</tr>
</thead>
<tbody>
<tr>
<td>320 x 240 (QVGA)</td>
<td>2</td>
<td>60</td>
<td>32</td>
<td>Full*</td>
</tr>
<tr>
<td>480 x 272 (WQVGA)</td>
<td>2</td>
<td>60</td>
<td>16</td>
<td>Full</td>
</tr>
<tr>
<td>480 x 272</td>
<td>1</td>
<td>60</td>
<td>32</td>
<td>Full</td>
</tr>
<tr>
<td>640 x 480 (VGA)</td>
<td>1</td>
<td>60</td>
<td>16</td>
<td>Good</td>
</tr>
<tr>
<td>640 x 480</td>
<td>1</td>
<td>60</td>
<td>32</td>
<td>Good</td>
</tr>
<tr>
<td>640 x 480</td>
<td>2</td>
<td>60</td>
<td>32</td>
<td>Limited</td>
</tr>
<tr>
<td>800 x 480 (WVGA)</td>
<td>2</td>
<td>60</td>
<td>16</td>
<td>Good</td>
</tr>
<tr>
<td>800 x 480</td>
<td>1</td>
<td>60</td>
<td>32</td>
<td>Good</td>
</tr>
<tr>
<td>800 x 480</td>
<td>2</td>
<td>60</td>
<td>32</td>
<td>Limited</td>
</tr>
<tr>
<td>800 x 600 (SVGA)</td>
<td>1</td>
<td>60</td>
<td>32</td>
<td>Very limited</td>
</tr>
</tbody>
</table>

Examples of display configurations supported by GLCDC

*Data buffer: on-chip memory*

![Diagram](image)
Segment LCD Controller (SLCDC) (3)

Generates AC voltage to drive an LCD screen based on the potential difference between common and segment signals
Provides up to 48 segment signals and 8 common signals
LCD driver voltage generation
  - External resistance division
  - External capacitor split
  - Internal voltage boosting
Automatic output of segment and common signals based on the contents of display data register
Hardware blink functionality
Contrast adjustment in 16 steps
Generates multiple waveforms to support variety of display types

<table>
<thead>
<tr>
<th>Pin Count</th>
<th>No. of Segment Signals</th>
<th>No. of Common Signals</th>
<th>No. Segments that can be driven</th>
</tr>
</thead>
<tbody>
<tr>
<td>144</td>
<td>48</td>
<td>8</td>
<td>384</td>
</tr>
<tr>
<td>120</td>
<td>34</td>
<td>8</td>
<td>272</td>
</tr>
<tr>
<td>100</td>
<td>22</td>
<td>8</td>
<td>176</td>
</tr>
</tbody>
</table>

Number of LCD signals for each pin count

Simplified implementation of Segment LCD Controller
2D Drawing Engine (DRW) (7,5)

Module to update the frame buffer with graphical content to off load CPU
Supports a variety of 2D graphics including lines, circles, ellipses, polygons, custom geometry, etc.

**Drawing Features**

**Vector Drawing**
- Allows for easier implementation of edge anti-aliasing and blurring with reduced overhead
- Uses half plane rendering approach
- Can be used to combine non-linear, quadratic equation-based primitives (conic sections, quadratic curves, etc.)

**BitBLT (Bit Boundary Block Transfer)**
- Allows combination of two bitmaps; for example, combining a rectangle and a texture.
- Results in fill, copy, rotate, scale, alpha blending, color conversion, bilinear filtering, etc.

Example of objects rendered by 2D Drawing Engine

Simplified rendering setup showing efficient decoupling of CPU (for other system tasks) & 2D Drawing Engine (for graphics rendering)
**JPEG Codec (7,5)**

On-chip JPEG Codec allows for high-speed compression of image data and decoding of JPEG data.
Conforms to JPEG baseline compression and decompression standard, JPEG Part 2, ISO-IEC 10918-2.
Block interleaved image input/output method.
4 quantization tables, 4 Huffman tables.
Output pixel format: ARGB8888, RGB565.

- **Compression**
  - YCbCr422 (H = 2:1:1, V = 1:1:1)

- **Decompression**
  - YCbCr444 (H = 1:1:1, V = 1:1:1)
  - 8 lines by 8 pixels minimum coded unit for each decompression
  - YCbCr422 (H = 2:1:1, V = 1:1:1)
  - 8 lines by 16 pixels MCU
  - YCbCr411 (H = 4:1:1, V = 1:1:1)
  - 8 lines by 32 pixels MCU
  - YCbCr420 (H = 2:1:1, V = 2:1:1)
  - 16 lines by 16 pixels MCU

Multiple markers supported:
- SOI (start of image), SOF0 (start of frame type 0), SOS (start of scan), DQT (define quantization tables), DHT (define Huffman tables), DRI (define restart interval), RSTm (restart marks), and EOI (end of image).
Parallel Data Capture (PDC) (7,5)

Peripheral to transfer parallel data (image output) from external I/O devices (image sensors) to Synergy MCU’s SRAM or external address space (SDRAM) via DTC or DMA
On-chip image handling
Wide range of parallel data capture
- Vertical: 1 line to 4095 lines
- Horizontal: 4 bytes to 4095 bytes
Operating frequency: 30 MHz*
VSYNC and HSYNC signal monitoring
Supports power consumption reduction function
Generates interrupt on multiple events

*If peripheral clock is 60 MHz
Security & Encryption

- 128-bit Unique ID
- TRNG
- AES (128/192/256)
- 3DES/DES/ARC4
- RSA
- SHA1/SHA224/SHA256
Secure Crypto Engine 7 (SCE7) (7,5)

Provides several security features and NIST-compliant, primitive cryptographic algorithms

Typical application use cases:
- Authentication and secure channel communication between the MCU and an external communication device
- Encryption of confidential and sensitive data for storage in the MCU

Typical application of security and encryption block

Simplified implementation of Secure Crypto Engine 7
Secure Crypto Engine 7 (7,5)

Unique ID
- 128-bit identification word unique per device
- Assigned by Renesas during manufacturing (can't be modified)
- Generates secure keys using a variety of encryption algorithms
- True RNG (TRNG)
- Generates cryptographically secure 128-bit random numbers at the rate of 0.1 Mbps to 5 Mbps
- Use as seed to other deterministic random number generators (such as the NIST SP800-90A DRBG)

Cryptographic Hash functions
- Generates hash values that provide a digital fingerprint of data

<table>
<thead>
<tr>
<th>Hash Function</th>
<th>Data Block Length*</th>
<th>Clock Cycles/Data Block</th>
</tr>
</thead>
<tbody>
<tr>
<td>SHA1</td>
<td>512 bits</td>
<td>80</td>
</tr>
<tr>
<td>SHA224, SHA256</td>
<td>512 bits</td>
<td>64</td>
</tr>
<tr>
<td>GHASH</td>
<td>128 bits</td>
<td>9</td>
</tr>
</tbody>
</table>

* Other data block lengths are also possible.

Throughput of generating hash functions

Simplified implementation of Secure Crypto Engine 7
Secure Crypto Engine 7 Symmetric Algo. (7,5)

Symmetric-key cryptography
- Encryption/decryption key that is secretly shared between transmitter and receiver

Advanced Encryption Standard (AES)
- Supports 128-bit, 192-bit, and 256-bit key lengths
- Supports various chaining modes: ECB, CBC, CTR, GCM, GCTR, and XTS
- Throughput for 128-bit data
  - For 128-bit key, 11 clocks/data block
  - For 256-bit key, 15 clocks/data block

3 Data Encryption Standard (3DES)
- Supports 56-bit key length, operates on a fixed 8-byte block of data
- Supports ECB and CBC chaining modes
- Used in legacy secure socket layer (SSL) and transport layer security (TLS) protocols
- Throughput for 64-bit data (for 3DES)
  - For 56-bit key, 16 clocks/data block

Alleged RC4 (ARC4)
- Supports 2048-bit key length
- Used in TLS and wired equivalent privacy (WEP)
- Throughput for 128-bit data
  - For 2048-bit key, 16 clocks/data block
Secure Crypto Engine 7 Asymmetric Algo. (7,5)

Public-key cryptography
- Generates two keys: public and private
- Transmitter encrypts using the public key
- Receiver decrypts using the private key
- Rivest, Shamir, and Adleman (RSA)
  - Supports up to 2048-bit key length
  - Used in digital verification for authentication, signature generation and verification, encryption/decryption for key exchange and wrapping, etc.
- Digital Signature Algorithm (DSA)
  - Supports up to 2048-bit key length
  - Used in authentication applications for digital signature generation and verification
  - Supports Diffie-Hellman key exchange
Secure Crypto Engine 5 (SCE5) (3)

Unique ID
- 128-bit unique identification word
- Generates secure keys using a variety of encryption algorithms
- Assigned by Renesas during manufacturing (can’t be modified)

True RNG (TRNG)
- Generates cryptographically secure 128-bit random numbers at 0.1 Mbps to 5 Mbps rate
- Use as seed to other deterministic random number generators (such as NIST SP800-90A DRBG)

Cryptographic GHASH function
- Used with AES-GCTR algorithm in authenticated encryption applications
- Throughput for 128-bit data
  - 33 clocks/data block

Advanced Encryption Standard (AES)
- Supports 128-bit and 256-bit key lengths
- Supports various chaining modes: ECB, CBC, CTR, GCTR, and XTS
- Throughput for 128-bit data
  - For 128-bit key, 44 clocks/data block
  - For 256-bit key, 61 clocks/data block
Security and Encryption (1)

Unique ID
- 128-bit unique identification word
- Generates secure keys using a variety of encryption algorithms
- Assigned by Renesas during manufacturing (can’t be modified)

True RNG (TRNG)
- Generates cryptographically secure 128-bit random numbers at 0.1 Mbps to 5 Mbps rate
- Use as seed to other deterministic random number generators (such as NIST SP800-90A DRBG)

Advanced Encryption Standard (AES)
- Supports 128-bit and 256-bit key lengths
- Supports various chaining modes: ECB, CBC, CTR, GCTR, and XTS
- Throughput for 128-bit data
  - For 128-bit key, 44 clocks/data block
  - For 256-bit key, 61 clocks/data block
Safety

- ECC in SRAM
- SRAM Parity Error Check
- Flash Area Protection
- ADC Diagnostics
- Clock Frequency Accuracy Measurement Circuit
- CRC Calculator
- Data Operation Circuit
- Port Output Enable Module for GPT
- IWDT
ECC in SRAM (7,5,3)

Mechanism to detect and correct the data corruption in a section of on-chip extended SRAM known as ECCRAM.
ECCRAM can be independently enabled or disabled:
- Disabled by default
Each user data is handled as 32-bit unit for ECC.
Error detection: 2-bit error
Error correction: 1-bit error
Available for a section on SRAM:
- Up to 32 KB in size
Interrupt generation upon error 1-bit or 2-bit error detection

Memory map of 640 KB SRAM with 32 KB ECCRAM
SRAM Parity Error Check (7,5,3,1)

Checks SRAM for parity errors upon reading
Adds single-bit parity bit to each 8-bit word in SRAM at the time of writing
Performs even parity check upon reading
Reset assertion or NMI generation upon error detection
Asserts an optional system reset upon error detection
Available for entire SRAM except ECCRAM*
Suitable for IEC 60730 Safety Standard for Household Appliances

SRAM Parity Error Check availability (example)

Write Operation

Read Operation

Simplified operation of SRAM Parity Error Check

* Not available on S1 series
**ADC Diagnostics (7,5,3,1)**

Self-diagnosis for the sample-and-hold circuit and the input multiplexer

- Multiple test voltages generated from the internal reference voltage are applied to the A/D Converter as one of its inputs
- The output of the ADC is compared against known good values to signal erroneous or improper operation of the input multiplexer or signal conversion in limited range
- ADC Diagnostics is executed once at the beginning of each scan

Suitable for IEC 60730 Safety Standard for Household Appliances
Can help improve reliability and quality

Example application: a fail-safe mechanism for temperature or rotor-positioning control

### Scanning Modes

- **Rotating Mode**
  - Three voltages, 0, VREFH/2 and VREFH are used for self diagnosis.
  - Allows for increased fault coverage.

- **Fixed Mode**
  - A fixed voltage is used for self diagnosis

---

ADC Diagnostics for sample and hold circuits and input multiplexers
ADC Diagnostics (7,5,3,1)

Input disconnect detection assist
- Allows for controlled charging/discharging of input circuit to effectively detect an input disconnection
- Discharging sample and hold (CADC) capacitor allows disconnected input to be read as 0
- Integrated functionality to pre-charge (pull up) and discharge (pull down) eliminates the need for an external discharging path and components
- Reduces complexity, system BOM cost, and PCB footprint

External voltage reference check
- Allows detecting unusual variations in the external reference voltage
- The internal reference voltage is periodically applied to the input of the ADC, and the output of the ADC is compared against a known good value.

Automatic data clearing
- ADC data register is cleared after it is read
- Prevents repeated reading of a “previous” value when the ADC is not converting in the absence of a trigger

[Diagram of ADC with annotations]

Input disconnect detection assist
Flash Area Protection (7,5,3,1)

Write-protects an area within the code flash to prevent undesired self-programming.
Access window can be configured in boot mode, self-programming mode, and debugger mode only.
Area protection can be enabled only during self-programming in single-chip mode per block basis.
Available for code flash only; not available for data flash.
Suitable for IEC 60730 Safety Standard for Household Appliances.

Example of Flash Area Protection

Note: Addresses shown in the diagram are device dependent.
**CRC Calculator (7,5,3,1)**

CRC code generator for error detection
Code is generated for 8 bits or 32 bits in parallel for data in 8n-bit or 32n-bit units
Selectable LSB-first or MSB-first
Snoop functionality
- Reads from and writes to specific addresses can be monitored for automatic CRC update
Variety of polynomials to choose from

<table>
<thead>
<tr>
<th>CRC generation Polynomials</th>
<th>8-bit</th>
<th>16-bit</th>
<th>32-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRC-8</td>
<td>(x^8 + x^2 + x + 1)</td>
<td>(x^{16} + x^15 + x^2 + 1)</td>
<td>(x^{32} + x^{28} + x^{27} + x^{26} + 25 + x^{23} + x^{22} + x^{20} + x^{19} + x^{18} + x^{16} + x^{13} + x^{11} + x^{10} + x^9 + x^6 + x^4 + x^3 + x^2 + x^1 + 1)</td>
</tr>
<tr>
<td>CRC-16</td>
<td>(x^{16} + x^{15} + x^2 + 1)</td>
<td>(x^{32} + x^{28} + x^{27} + x^{26} + 25 + x^{23} + x^{22} + x^{20} + x^{19} + x^{18} + x^{16} + x^{13} + x^{11} + x^{10} + x^9 + x^6 + x^4 + x^3 + x^2 + x^1 + 1)</td>
<td></td>
</tr>
<tr>
<td>CRC-CCITT</td>
<td>(x^{16} + x^{12} + x^8 + 1)</td>
<td>(x^{32} + x^{28} + x^{27} + x^{26} + 25 + x^{23} + x^{22} + x^{20} + x^{19} + x^{18} + x^{16} + x^{13} + x^{11} + x^{10} + x^9 + x^6 + x^4 + x^3 + x^2 + x^1 + 1)</td>
<td></td>
</tr>
</tbody>
</table>

Simplified implementation of the CRC Calculator
Clock Frequency Accuracy Measurement Circuit (CAC) (7,5,3,1)

Checks the system clock frequency based on a reference clock for accuracy.
Counts the number of pulses of the measurement clock within the time generated by reference clock.
Suitable for IEC 60730 Safety Standard for Household Appliances to implement a failsafe mechanism.
Multiple interrupt outputs.

Reference Clock Sources

**Internal**
1. Main clock oscillator
2. Sub-clock oscillator ($f_{sub}$)
3. High-Speed On-Chip Oscillator (HOCO)
4. Middle-Speed On-Chip Oscillator (MOCO)
5. Low-Speed On-Chip Oscillator (LOCO)
6. Peripheral module clock (PCLKB)
7. Independent watchdog timer clock

**External**
Applied through CACREF pin.

Simplified implementation of the Clock Frequency Accuracy Measurement Circuit.
Data Operation Circuit (DOC) (7,5,3,1)

Dedicated hardware to perform 16-bit addition, subtraction, and comparison without CPU intervention
Specifically reduces CPU load while performing memory tests
Suitable for IEC 60730 Safety Standard for Household Appliances
Interrupt generation on multiple events based on the result of data operation
Event Link Controller function output
Example applications:
- Smart refrigerators
- Smart dishwashers
- Smart cooking products
- Smart washer and dryers
- Smart HVAC
- Smart building control

Simplified implementation of the Data Operation Circuit
Independent Watchdog Timer (IWDT) (7,5,3,1)

Independent watchdog timer with a dedicated low-speed clock source

**Auto-Start Mode**
Counting automatically starts after reset. Initialization options:
1) Clock frequency division ratio after a reset
2) Timeout period
3) Window start or end position
5) Reset output or interrupt request
6) Down-count stop function at transition to a low power mode

**Start Conditions**
- **Reset**
  - Down-counter and other registers return to their initial values

**Stop Conditions**
- **Underflow or Refresh Error**
  - Counter underflows or a refresh error is generated

14-bit down counter supports clock division by 16, 32, 64, 128, and 256
Supports window functionality
Event Link Controller function output
Issues reset or non-maskable interrupt on down-counter underflow and refresh error
## Comparison Between Watchdog Timers (7,3,5,1)

<table>
<thead>
<tr>
<th>Features</th>
<th>Watchdog Timer</th>
<th>Independent Watchdog Timer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Counter Operation</strong></td>
<td>14-bit down counter</td>
<td>14-bit down counter</td>
</tr>
<tr>
<td><strong>Count Source</strong></td>
<td>Peripheral clock (PCLK)</td>
<td>IWDT-dedicated clock (IWDTCLK)</td>
</tr>
<tr>
<td><strong>Counter Stop Conditions</strong></td>
<td>Auto-start* (after a reset/after a underflow/refresh error occurs) Register start (writing to register)</td>
<td>Auto start* after a reset</td>
</tr>
<tr>
<td><strong>Counter Start Conditions</strong></td>
<td>Reset A counter underflows or refresh error is generated</td>
<td>Reset A counter underflows or refresh error is generated</td>
</tr>
<tr>
<td><strong>Window Functionality</strong></td>
<td>Available</td>
<td>Available</td>
</tr>
<tr>
<td><strong>Reset Sources</strong></td>
<td>Down counter underflows Refresh error</td>
<td>Down counter underflows Refresh error</td>
</tr>
<tr>
<td><strong>Non-Maskable Interrupt sources</strong></td>
<td>Down counter underflows Refresh error</td>
<td>Down counter underflows Refresh error</td>
</tr>
<tr>
<td><strong>Event Link Function (output)</strong></td>
<td>-</td>
<td>Available</td>
</tr>
<tr>
<td><strong>Available In</strong></td>
<td>S7 S5 S3 S1</td>
<td>S7 S5 S3 S1</td>
</tr>
</tbody>
</table>

*Need Initialization
Port Output Enable Module for GPT (POEG) (7,5,3,1)

Can disable timer output pins in response to several events in order to implement safety mechanisms

- Comparator Interrupt Detection
  Upon change of comp. op. result

- Disable Request From Timers
  Upon detection of dead time error

- Input Level Detection
  By sampling GTETRGA…D pins

- Oscillator Stop Detection
  By setting registers

- Software
  By setting registers

Event Link Controller function output
Suitable for IEC 60730 Safety Standard for Household Appliances

Simplified implementation of
Port Output Enable Module for GPT
Package Navigator

Click on the check box to view package details.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Pin Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>LGA</td>
<td>36, 40, 48, 64, 100, 121, 144, 145, 176, 224</td>
</tr>
<tr>
<td>QFN</td>
<td>36, 40, 48, 64, 100, 121, 144, 145, 176, 224</td>
</tr>
<tr>
<td>LQFP</td>
<td>36, 40, 48, 64, 100, 121, 144, 145, 176, 224</td>
</tr>
<tr>
<td>BGA</td>
<td>36, 40, 48, 64, 100, 121, 144, 145, 176, 224</td>
</tr>
</tbody>
</table>
**LGA-36**

<table>
<thead>
<tr>
<th>JEITA Package Code</th>
<th>Renesas Code</th>
<th>Previous Code</th>
<th>Mass (typ. g)</th>
<th>Package Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-WFLGA36-4x4-0.50</td>
<td>PWLG0036KA-A</td>
<td>P36FC-50-AA4-2</td>
<td>0.023</td>
<td>LM</td>
</tr>
</tbody>
</table>

**Reference Symbol** | **Dimension (typ. mm)**
---|---
D | 4.0
E | 4.0
w | 0.20
| | 0.50
A | 0.69
b | 0.24
x | 0.05
y | 0.08
y₁ | 0.20
ZD | 0.75
ZE | 0.75

**Package drawing**
# LGA-100

<table>
<thead>
<tr>
<th>JEITA Package Code</th>
<th>Renesas Code</th>
<th>Previous Code</th>
<th>Mass (typ. g)</th>
<th>Package Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-TFLGA100-7x7-0.65</td>
<td>PTLG0100JA-A</td>
<td>100F0G</td>
<td>0.1</td>
<td>LA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Reference Symbol</th>
<th>Dimension (typ. mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>7.0</td>
</tr>
<tr>
<td>E</td>
<td>7.0</td>
</tr>
<tr>
<td>v</td>
<td>0.15 (max)</td>
</tr>
<tr>
<td>w</td>
<td>0.20 (max)</td>
</tr>
<tr>
<td>A</td>
<td>1.06 (max)</td>
</tr>
<tr>
<td>e</td>
<td>0.65</td>
</tr>
<tr>
<td>b</td>
<td>0.35</td>
</tr>
<tr>
<td>b₁</td>
<td>0.435</td>
</tr>
<tr>
<td>x</td>
<td>0.08 (max)</td>
</tr>
<tr>
<td>y</td>
<td>0.1 (max)</td>
</tr>
<tr>
<td>Z₀</td>
<td>0.575</td>
</tr>
<tr>
<td>Zₑ</td>
<td>0.575</td>
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**Package drawing**
# LGA-145

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<tbody>
<tr>
<td>P-TFLGA145-7x7-0.50</td>
<td>PTLG0145KA-A</td>
<td>145F0G</td>
<td>0.1</td>
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## Package Dimensions

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<th>Dimension (typ. mm)</th>
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<tr>
<td>D</td>
<td>7.0</td>
</tr>
<tr>
<td>E</td>
<td>7.0</td>
</tr>
<tr>
<td>v</td>
<td>0.15 (max)</td>
</tr>
<tr>
<td>w</td>
<td>0.20 (max)</td>
</tr>
<tr>
<td>A</td>
<td>1.05 (max)</td>
</tr>
<tr>
<td>e</td>
<td>0.5</td>
</tr>
<tr>
<td>b</td>
<td>0.25</td>
</tr>
<tr>
<td>b₁</td>
<td>0.34</td>
</tr>
<tr>
<td>x</td>
<td>0.08 (max)</td>
</tr>
<tr>
<td>y</td>
<td>0.1 (max)</td>
</tr>
<tr>
<td>Z₀</td>
<td>0.5</td>
</tr>
<tr>
<td>Zₑ</td>
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## Package Drawing

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QFN-40

<table>
<thead>
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<th>Previous Code</th>
<th>Mass (typ, g)</th>
<th>Package Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-HWQFN40-6x6-0.50</td>
<td>PWQN0040KC-A</td>
<td>P40K8-50-4B4-5</td>
<td>0.09</td>
<td>NF</td>
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Reference Symbol | Dimension (typ, mm) |
--- | --- |
D | 6.0 |
E | 6.0 |
A | 0.80 (max) |
A₁ | 0 |
b | 0.25 |
e | 0.50 |
Lp | 0.40 |
x | 0.05 (max) |
y | 0.05 (max) |
Z₀ | 0.75 |
Zₑ | 0.75 |
c₂ | 0.20 |
D₂ | 4.50 |
E₂ | 4.50 |

Package dimensions
# QFN-48

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<th>Previous Code</th>
<th>Mass (typ, g)</th>
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<tbody>
<tr>
<td>P-HWQFN48-7x7-0.50</td>
<td>PWQN0048KB-A</td>
<td>48PJN-A, P48K8-50-5B4-6</td>
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## Reference Symbol and Dimension (typ, mm)

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</tr>
<tr>
<td>E</td>
<td>7.0</td>
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<tr>
<td>A</td>
<td>0.80 (max)</td>
</tr>
<tr>
<td>A₁</td>
<td>0</td>
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<tr>
<td>b</td>
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<tr>
<td>e</td>
<td>0.50</td>
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<tr>
<td>L_p</td>
<td>0.40</td>
</tr>
<tr>
<td>x</td>
<td>0.05 (max)</td>
</tr>
<tr>
<td>y</td>
<td>0.05 (max)</td>
</tr>
<tr>
<td>Z_D</td>
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<tr>
<td>Z_E</td>
<td>0.75</td>
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<tr>
<td>c₁</td>
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<tr>
<td>D₂</td>
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<tr>
<td>E₂</td>
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## Package drawing

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## QFN-64

<table>
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<tr>
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<th>Mass (typ. g)</th>
<th>Package Type</th>
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<tbody>
<tr>
<td>P-HWQFN64-8x8-0.40</td>
<td>PWQN0064LA-A</td>
<td>P64K8-40-9B5-3</td>
<td>0.16</td>
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### Package drawing

**Package dimensions**

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<tr>
<td>E</td>
<td>8.0</td>
</tr>
<tr>
<td>A</td>
<td>0.80 (max)</td>
</tr>
<tr>
<td>A₁</td>
<td>0</td>
</tr>
<tr>
<td>b</td>
<td>0.20</td>
</tr>
<tr>
<td>e</td>
<td>0.40</td>
</tr>
<tr>
<td>Lₚ</td>
<td>0.40</td>
</tr>
<tr>
<td>x</td>
<td>0.05 (max)</td>
</tr>
<tr>
<td>y</td>
<td>0.05 (max)</td>
</tr>
<tr>
<td>Z₀</td>
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</tr>
<tr>
<td>Zₑ</td>
<td>1.00</td>
</tr>
<tr>
<td>c₂</td>
<td>0.20</td>
</tr>
<tr>
<td>D₂</td>
<td>6.50</td>
</tr>
<tr>
<td>E₂</td>
<td>6.50</td>
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</table>
### LQFP-48

#### JEITA Package Code | Renesas Code | Previous Code | Mass (typ, g) | Package Type
---|---|---|---|---
P-LFQFP48-7x7-0.50 | PLQP0048KB-A | 48P6Q-A | 0.2g | FL

#### Reference Symbol | Dimension (typ, mm)
---|---
D | 7.0
E | 7.0
A₂ | 1.4
H₃ | 9.0
HE | 9.0
A | 1.7 (max)
A₁ | 0.1
b₂ | 0.22
b₁ | 0.20
c | 0.145
c₁ | 0.125
Θ | 8 (max)
e | 0.5
x | 0.08 (max)
y | 0.10 (max)
Z₀ | 0.75
Zₑ | 0.75
L | 0.5
L₁ | 1.0

**Package drawing**

Note:
1. Dimension "1" and "2" do not include mold flash
2. Dimension "3" does not include trim offset
# LQFP-64

<table>
<thead>
<tr>
<th>JEITA Package Code</th>
<th>Renesas Code</th>
<th>Previous Code</th>
<th>Mass (typ. g)</th>
<th>Package Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-LFQFP-10x10-0.50</td>
<td>PLQP0064KB-A</td>
<td>64P6Q-A/FP-64K/FP-64KV</td>
<td>0.3</td>
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## Package drawing

### Reference Symbol

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<th>Reference Symbol</th>
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<td>E</td>
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<td>A²</td>
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<td>H_D</td>
<td>12.0</td>
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<tr>
<td>H_E</td>
<td>12.0</td>
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<tr>
<td>A</td>
<td>1.7 (max)</td>
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<tr>
<td>Z1</td>
<td>0.1</td>
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<td>b_p</td>
<td>0.20</td>
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<tr>
<td>b_1</td>
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<tr>
<td>c</td>
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<tr>
<td>c_1</td>
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</tr>
<tr>
<td>Θ</td>
<td>8° (max)</td>
</tr>
<tr>
<td>Ε</td>
<td>0.5</td>
</tr>
<tr>
<td>x</td>
<td>0.08 (max)</td>
</tr>
<tr>
<td>y</td>
<td>0.08 (max)</td>
</tr>
<tr>
<td>Z0</td>
<td>1.25</td>
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<td>Z_E</td>
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<tr>
<td>L</td>
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<td>L_1</td>
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### Package dimensions

Note:
1. Dimension "1" and "2" do not include mold flash
2. Dimension "3" does not include trim offset
### Reference Symbol

<table>
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### JEITA Package Code

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<th>Previous Code</th>
<th>Mass (typ, g)</th>
<th>Package Type</th>
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<tbody>
<tr>
<td>P-LFQFP100-14x14-0.50</td>
<td>PLQP0100KB-A</td>
<td>100P6Q-A/FP-100U/FP-100UV</td>
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### Package drawing

Note:
1. Dimension "*1" and "*2" do not include mold flash
2. Dimension "*3" does not include trim offset
LQFP-144

<table>
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<tr>
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<th>Renesas Code</th>
<th>Previous Code</th>
<th>Mass (typ, g)</th>
<th>Package Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-LFQFP144-20x20-0.50</td>
<td>PLQP0144KA-A</td>
<td>144P6Q-A/FP-144L/FP-144LV</td>
<td>1.2</td>
<td>FB</td>
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**Reference Symbol**

<table>
<thead>
<tr>
<th>Reference Symbol</th>
<th>Dimension (typ, mm)</th>
</tr>
</thead>
<tbody>
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<td>E</td>
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<tr>
<td>A2</td>
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<td>H_E</td>
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<tr>
<td>A1</td>
<td>0.1</td>
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<tr>
<td>b_p</td>
<td>0.22</td>
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<tr>
<td>b_1</td>
<td>0.20</td>
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<tr>
<td>c</td>
<td>0.145</td>
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<tr>
<td>c_1</td>
<td>0.125</td>
</tr>
<tr>
<td>Θ</td>
<td>8° (max)</td>
</tr>
<tr>
<td>e</td>
<td>0.5</td>
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<tr>
<td>x</td>
<td>0.08 (max)</td>
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<tr>
<td>y</td>
<td>0.01 (max)</td>
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<tr>
<td>Z_D</td>
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<tr>
<td>Z_E</td>
<td>1.25</td>
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<tr>
<td>L</td>
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<tr>
<td>L_1</td>
<td>1.0</td>
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**Package drawing**

**Package dimensions**

**Note:**
1. Dimension "1" and "2" do not include mold flash
2. Dimension "3" does not include trim offset
# LQFP-176

<table>
<thead>
<tr>
<th>JEITA Package Code</th>
<th>Renesas Code</th>
<th>Previous Code</th>
<th>Mass (typ, g)</th>
<th>Package Type</th>
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<tbody>
<tr>
<td>P-LFQFP176-24x24-0.50</td>
<td>PLQP0176KB-A</td>
<td>176P6Q-A/FP-176E/FP-176EV</td>
<td>1.8</td>
<td>FC</td>
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## Package dimensions

Note:
1. Dimension "1" and "2" do not include mold flash
2. Dimension "3" does not include trim offset
# BGA-121

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<tr>
<td>P-TFBGA121-8X8-0.65</td>
<td>PTBG0121JB-A</td>
<td>P121F1-65-CA7-2</td>
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### Package drawing

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<tr>
<td>E</td>
<td>8.00</td>
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<td>A2</td>
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<tr>
<td>b</td>
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<tr>
<td>x</td>
<td>0.08</td>
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<tr>
<td>y</td>
<td>0.10</td>
</tr>
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<td>y1</td>
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<td>ZD</td>
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**BGA-176**

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<tbody>
<tr>
<td>P-FBGA176-13x13-0.80</td>
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**Reference Symbol**

<table>
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<tr>
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<td>0.15 (max)</td>
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<tr>
<td>w</td>
<td>0.20 (max)</td>
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<td>A</td>
<td>1.9 (max)</td>
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**Package drawing**
BGA-224

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<tr>
<td>P-LFBGA224-13x13-0.80</td>
<td>PLBG0224GA-A</td>
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<table>
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<tr>
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<tr>
<td>Ze</td>
<td>0.9</td>
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Package dimensions

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